Reconfigurable Architectures

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Reconfigurable System (Custom Computing Machine)

- A target algorithm is executed directly with a hardware on SRAM-style FPGA/PLDs.
  - High performance of special purpose machines.
  - High degree of flexibility of general purpose machines.
- A completely different execution mechanism from stored program computers.

PLD（Programmable Logic Device）

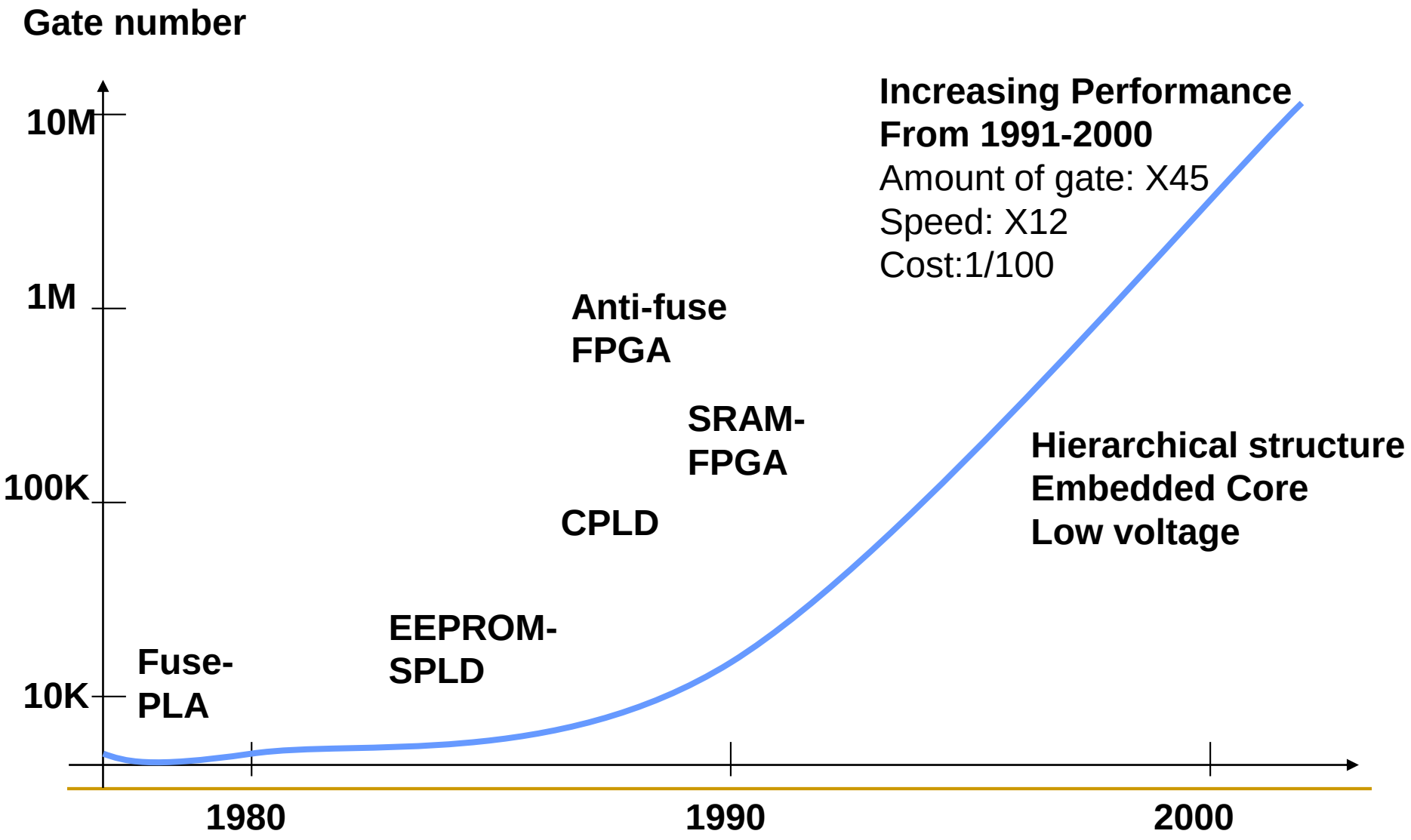
- Integrated Circuit whose logic function can be defined by users.

⟷ Standard IC, ASIC(Application Specific IC)

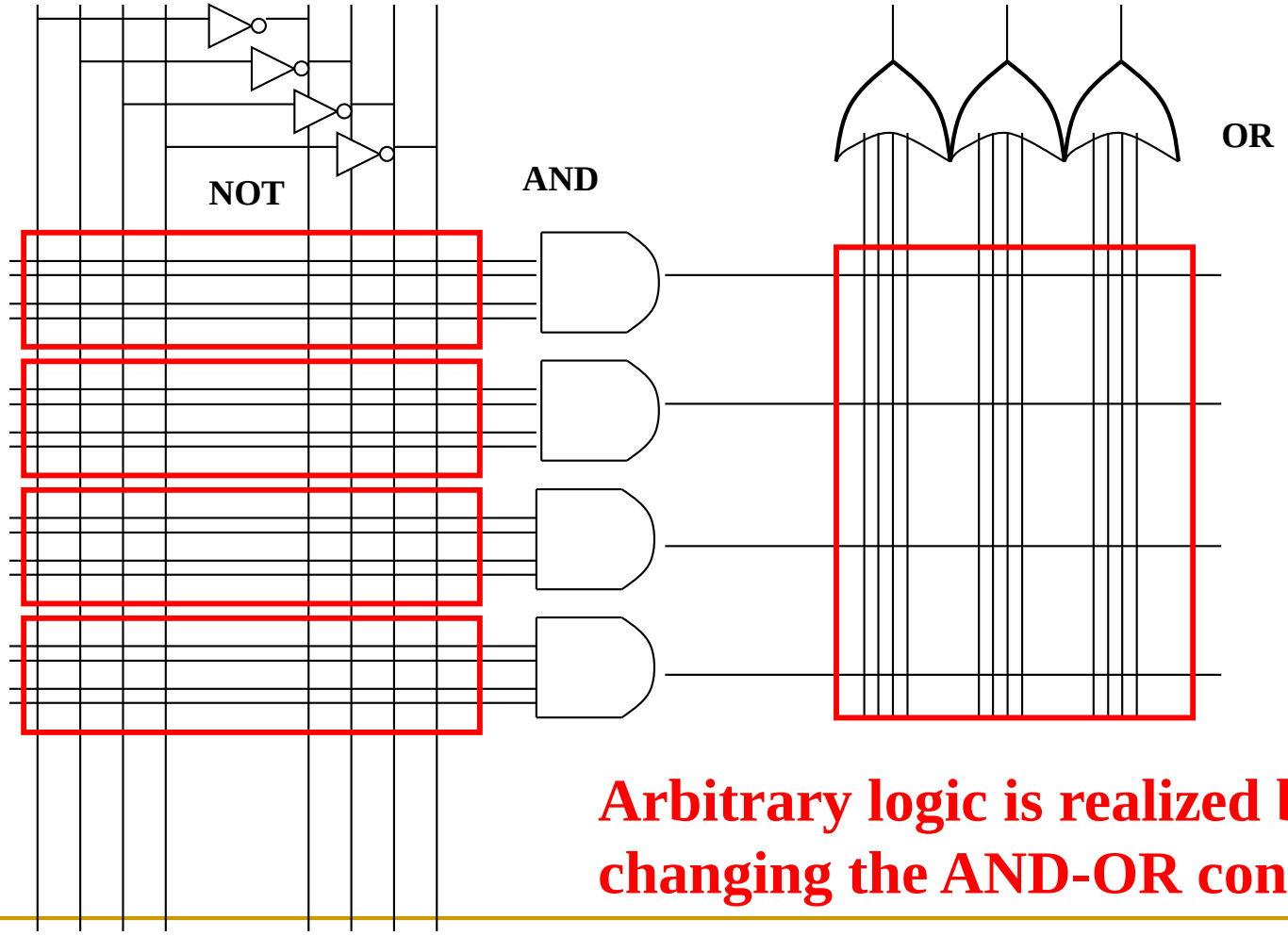
- SPLD（Simple PLD) / PLA（Programmable Logic Array)
  - Small scale IC with AND-OR array
- CPLD(Complex PLD)
  - Middle scale IC with AND-OR array
- FPGA（Field Progarmmable Gate Array）
  - Large scale IC with LUT

Caution! Terms are not well defined!

Rapidly development of PLD

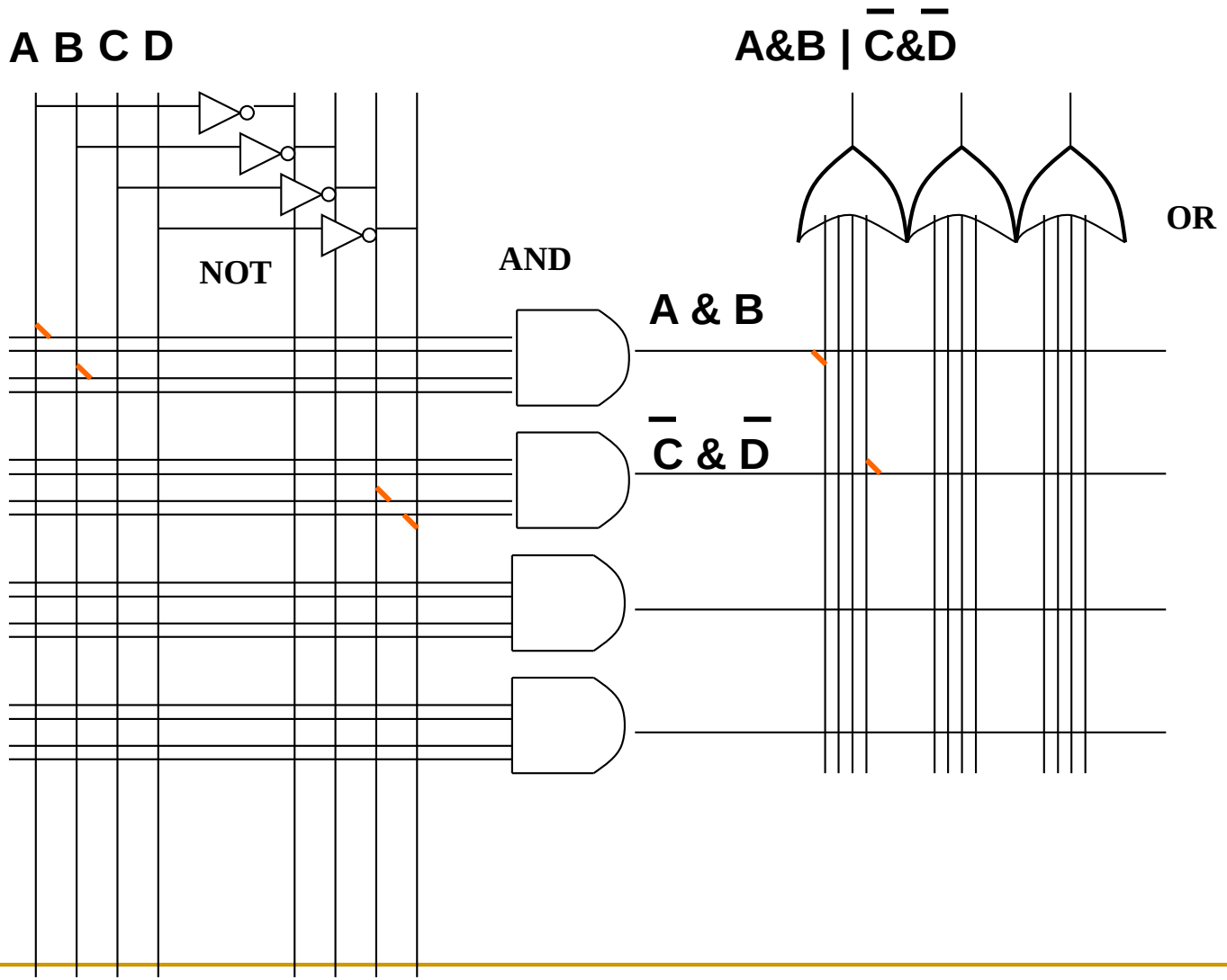


SPLD（Simple PLD: AND-OR/Product-term）

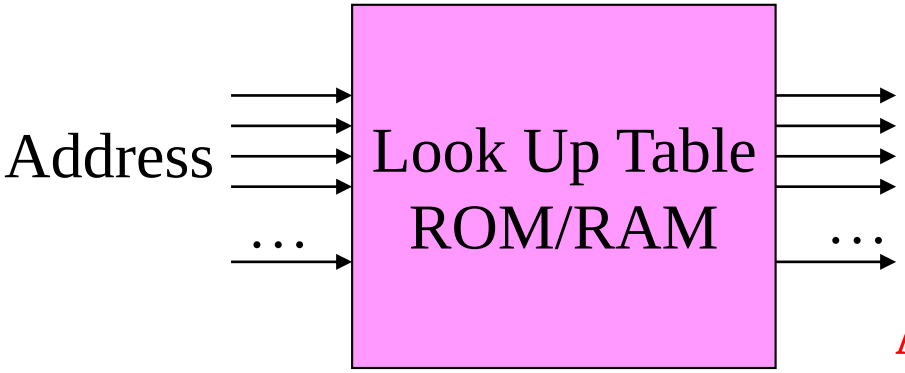


Arbitrary logic is realized by changing the AND-OR connection

AND/OR connection example

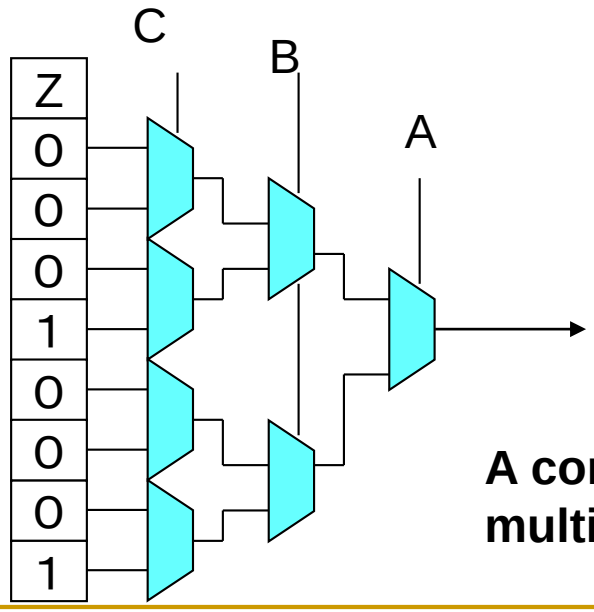


LUT : Look Up Table



A simple ROM/RAM can used as a random logic.

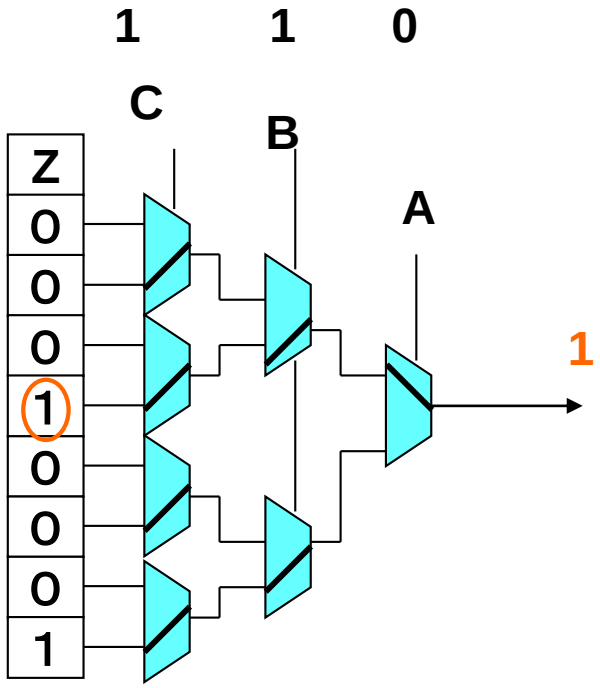
ABC	Z
000	0
001	0
010	0
011	1
100	0
101	0
110	0
111	1



A combination of memory and multiplexers are commonly used.

An example using LUT : Look Up Table

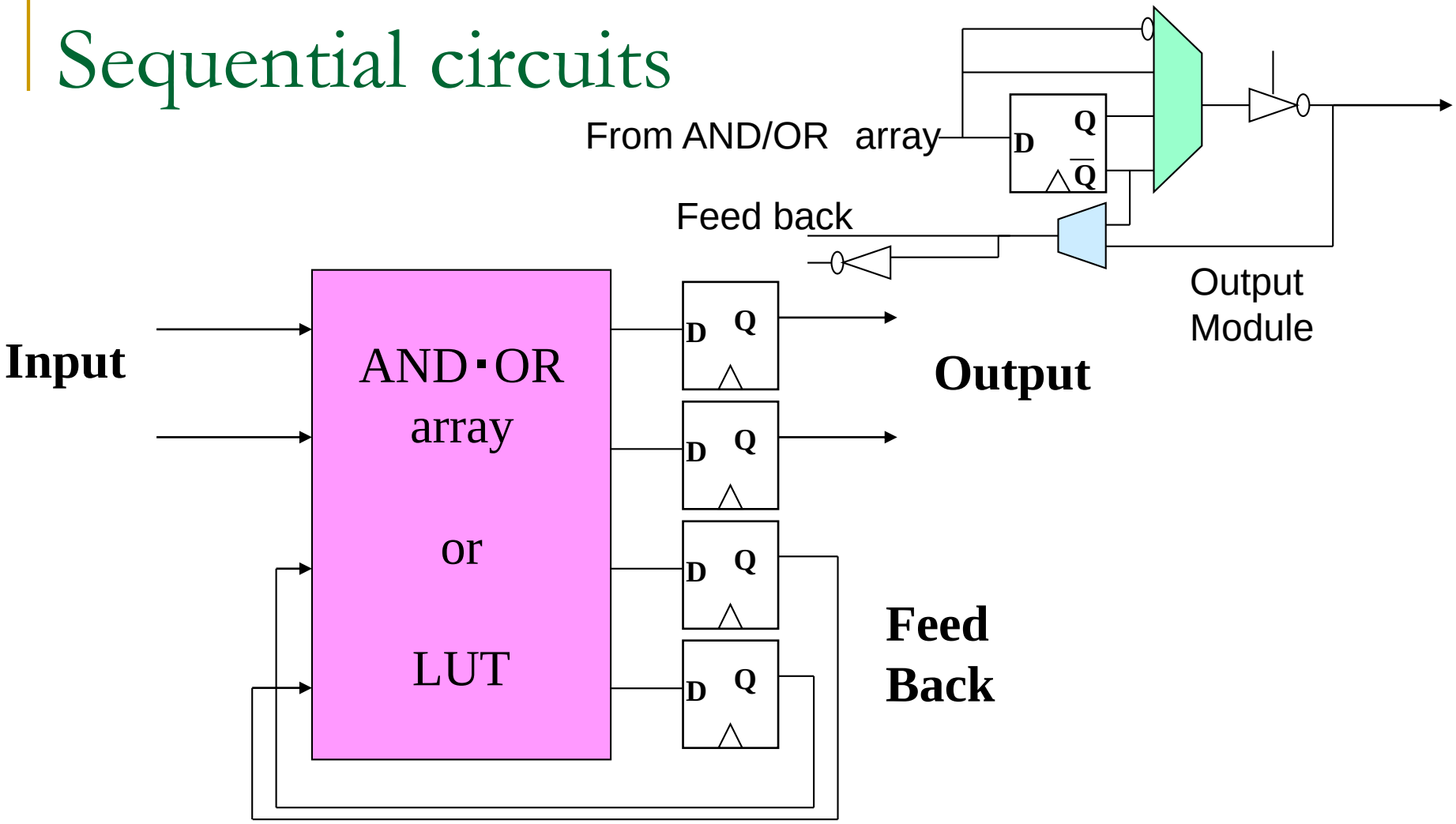
ABC	Z
000	0
001	0
010	0
011	1
100	0
101	0
110	0
111	1



AND-OR array vs. LUT

- AND-OR array（product-term）
  - Efficient for logic with multiple outputs
  - There is a type of logic which cannot be realized.
  - Suitable for EEPROM and Flash-ROM
- LUT
  - Any logic can be realized.
  - Efficient for logic with a single output
  - Suitable for Flash-ROM, Anti-fuse, and SRAM.

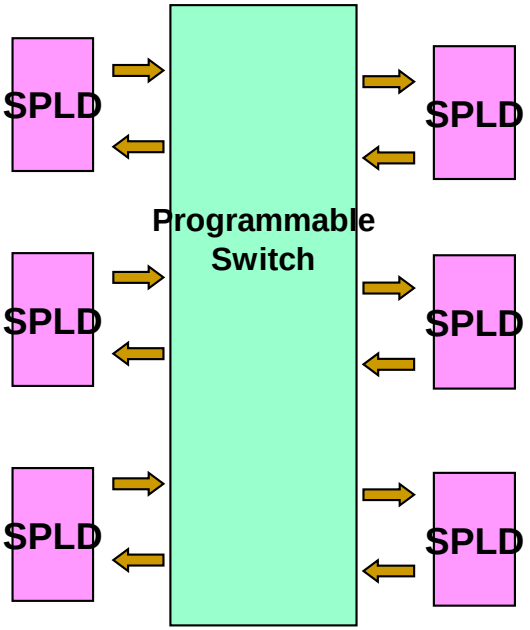
Sequential circuits



Sequential circuit (state machine) can be built by attaching Flip-flops and feed back loops.

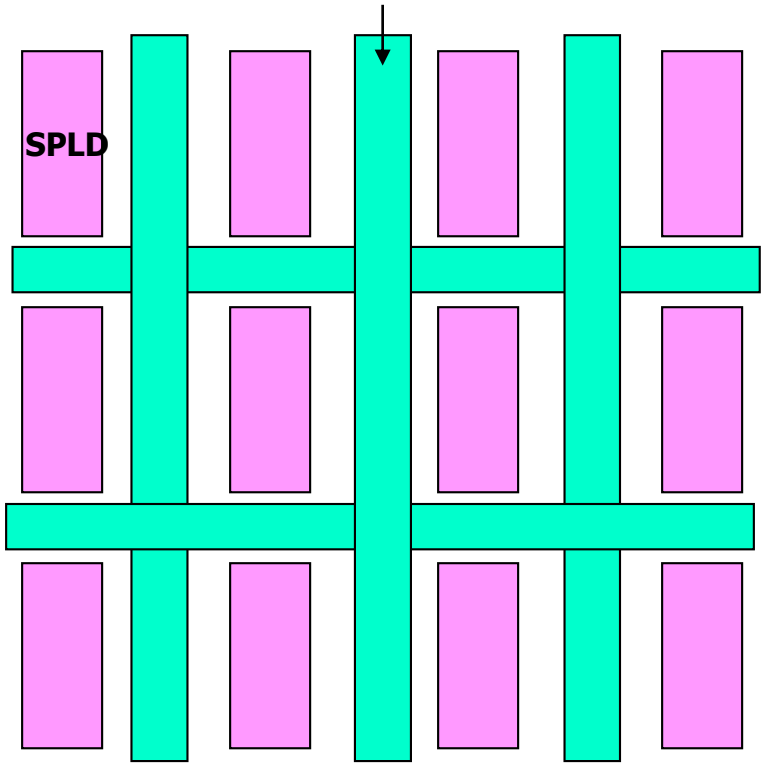
CPLD (Complex PLD)

Matrix of SPLDs



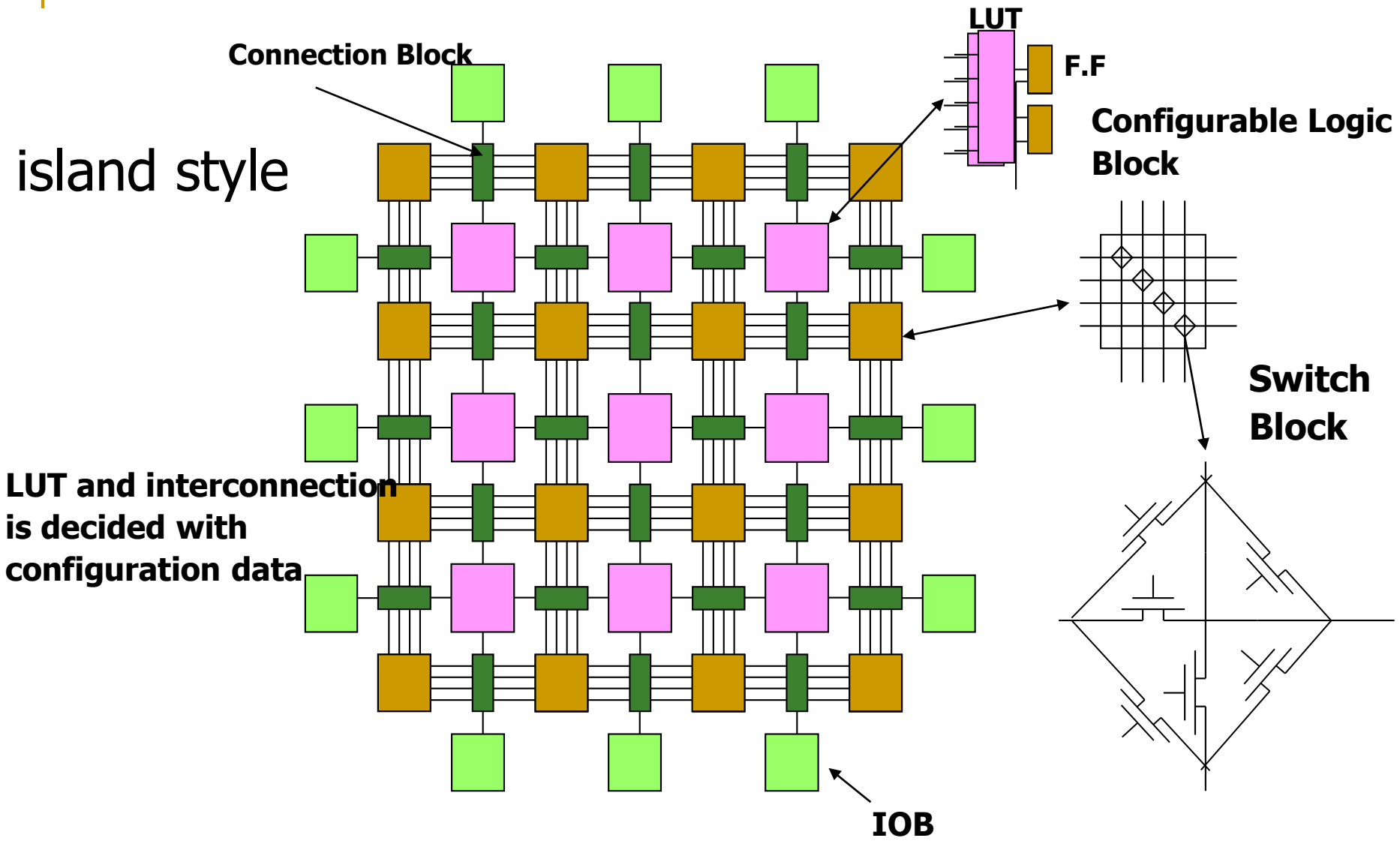
Altera's MAX

Programmable Switch



2-dimensional Array

FPGA(Field Programmable Gate Array)



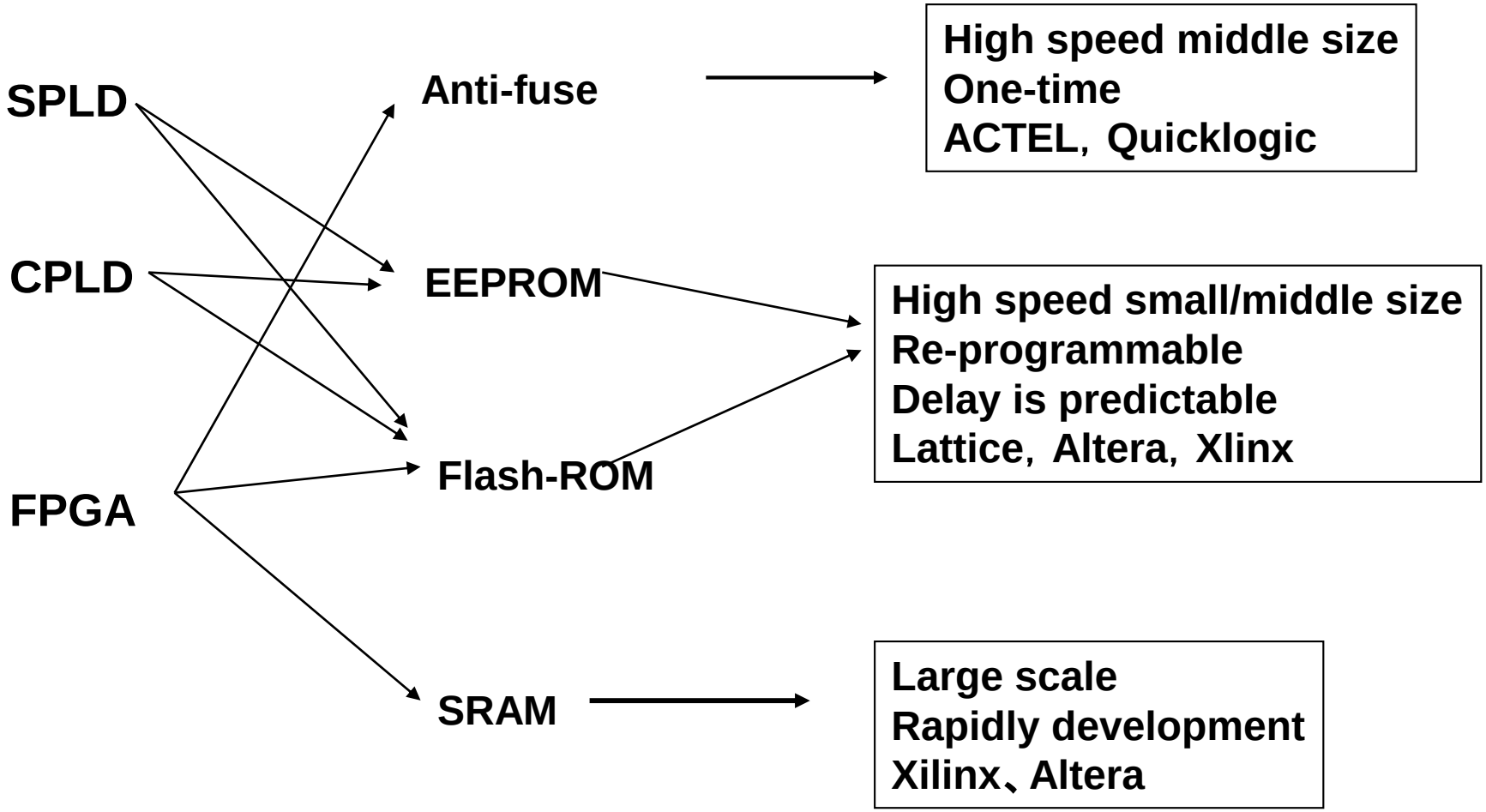
Device for flexibility（1）

- Anti-fuse type
  - Program by destruction of isolation with high voltage
  - High speed but One-time
  - ACTEL、Quicklogic
- EEPROM・Flash-ROM
  - Switches for connections are realized by floating gates.
  - Re-programmable
  - Lattice、Altera’s MAX series

Device for flexibility(2)

- SRAM
  - Data on SRAM represents look up table and wire connection.
  - ISP (In System Programming) is available.
  - The configuration data is erased, when the power turns off.
  - Suitable for a large scale FPGA. Recently, rapidly advanced.
  - Xilinx XC、 Altera FLEX, Lucent ORCA
  - The advanced series: Xilinx Virtex, Altera Stratix
- その他
  - Magnetic memory
  - DRAM

Architectures and devices



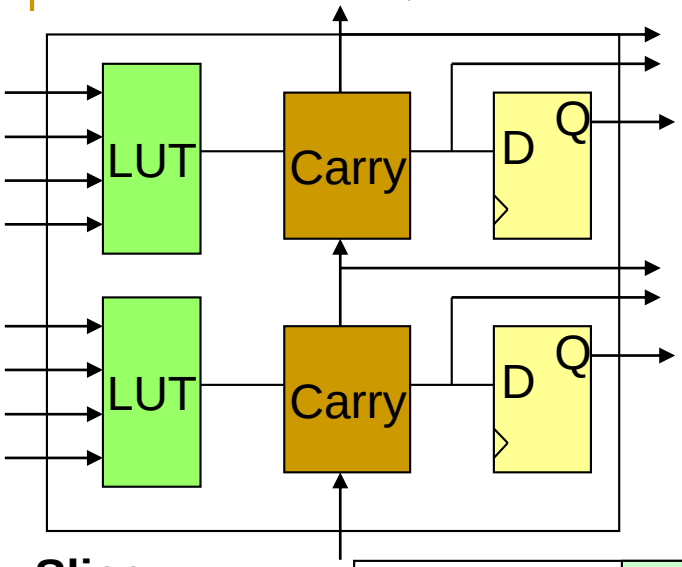
Recent PLDs

- High-end: a large scale chip with hierarchical structure：
  - Xilinx's Virtex II、Virtex-4/LX, Altera's Stratix-3
  - System on Programmable Device
  - Providing DLL, CPU、DSP, ROM, RAM, Multiplier, High speed link, and other hard IPs.
  - Xilix's Virtex-4/EX,FX, Altera's Stratix-3
- Specialized for mass-production
  - Low cost：Xilinx's Spartan, Altera's Cyclone
- Low voltage, Multiple voltages, and Low power consumption

Process and parameters（Xilinx co.）

Process	Products	Name	LUT	Power
350nm	XC4000	XC4085KLA	7448	3.3V
250nm	XC4000	XC40250KV	20102	2.5V
220nm	Virtex	XCV1000	27648	2.5V
180nm	Virtex-E	XCV2000E	43200	1.8V
150nm	Virtex-II	XC2V800O	104882	1.5V
130nm	Virtex-II Pro	XC2VP125	125136	1.5V
90nm	Virtex-4	XC4VLX200	200488	1.2V
65nm	Virtex-5	XC5VLX330	51840slice	1.0V
40nm	Virtex-6	XC6VLX760	118560slice	1.0V
28nm	Virtex-7	XC7VX1140T	1139200slice	0.9V

Xilinx Virtex II



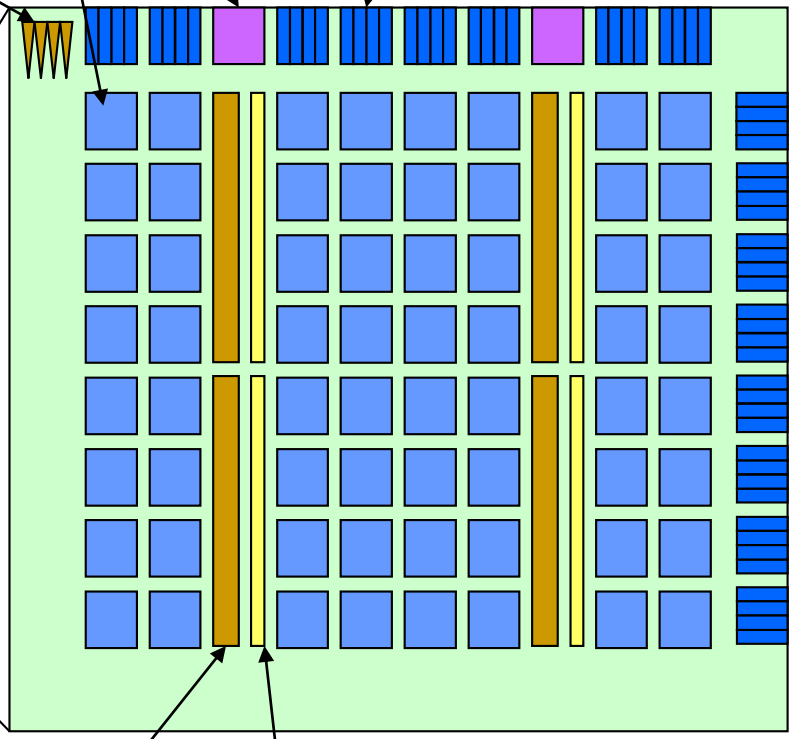
Slice

Slice X 2 → CLB (Configurable Logic Block)

Global Clock MUX

DCM

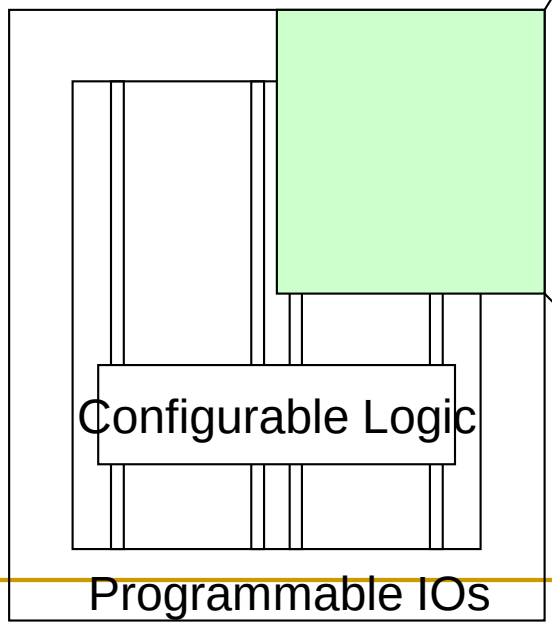
IOB



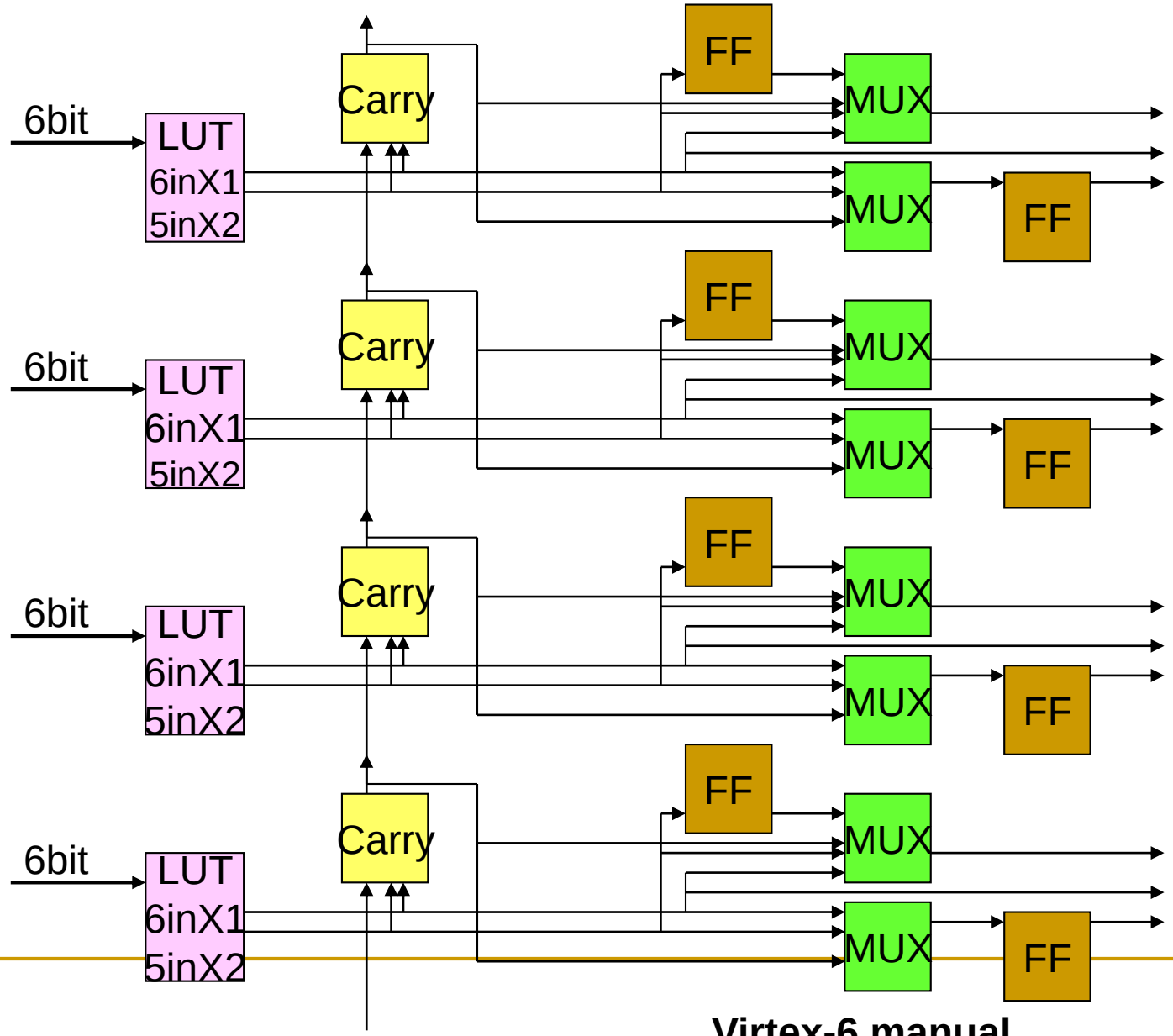
RAM

Multiplier

100000 CLBs
3Mbit

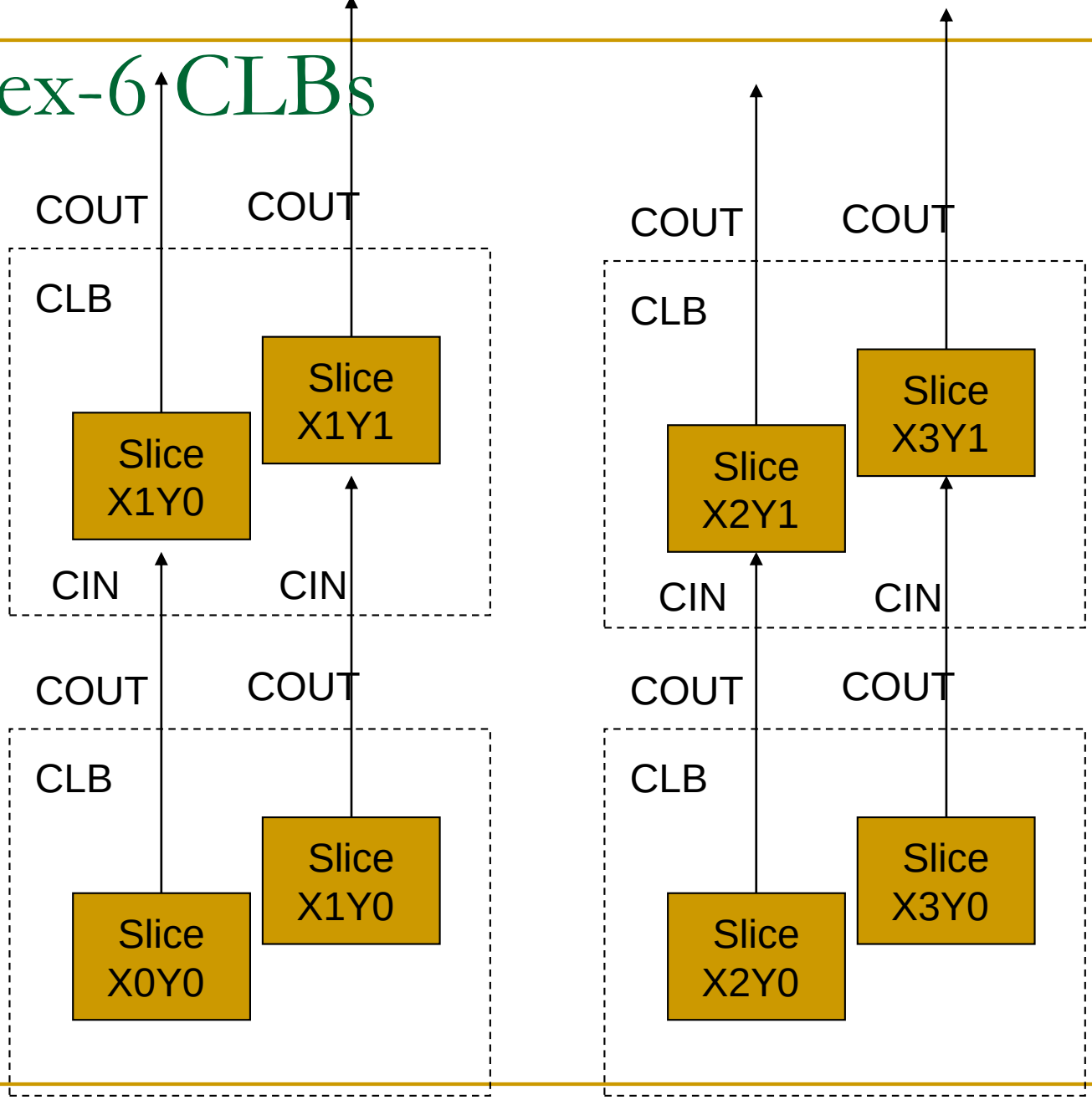


Slice structure of Virtex-6



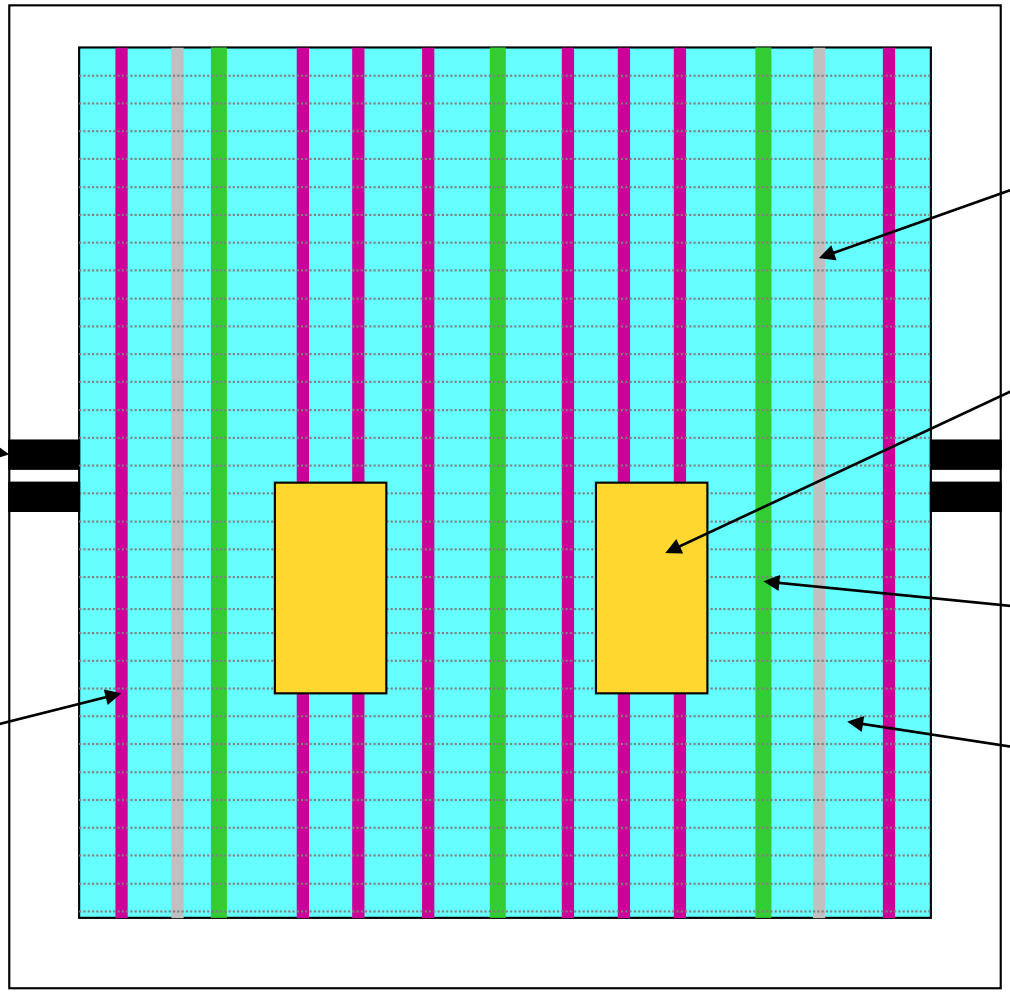
Virtex-6 manual

Virtex-6 CLBs



Virtex-6 manual

Altera Stratix II



DSP Blocks

Mega RAM Blocks

M4K RAM Blocks

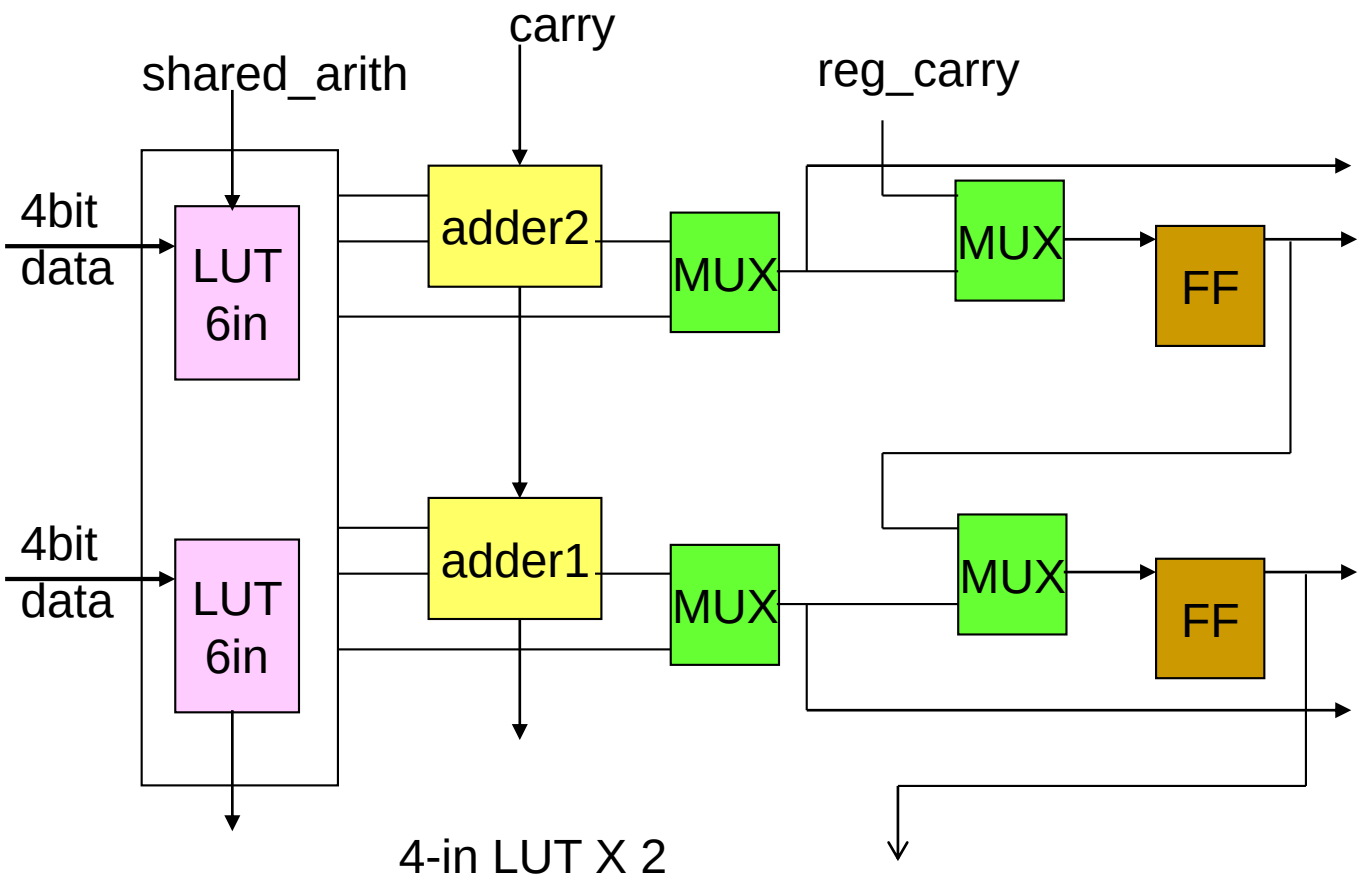
LAB : Logic Array Block consisting of 10 LE (4-input LUT and F.F.)

Hierarchical Interconnect

PLL

M512 RAM Blocks

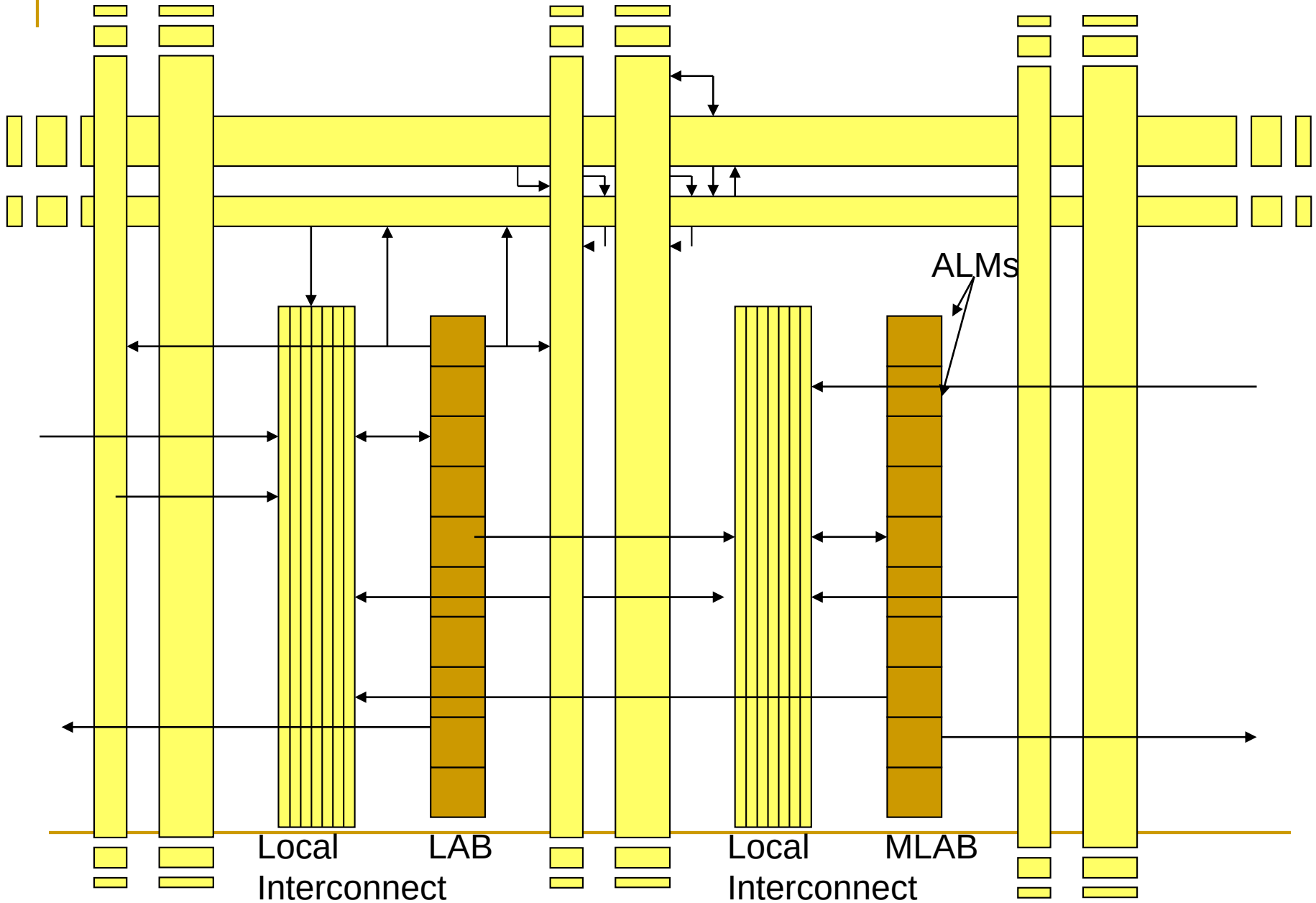
Stratix-IV ALM Structure



4-in LUT X 2
5-in LUT + 3-in LUT
5-in LUT + 4-in LUT 1-input shared
5-in LUT + 5-in LUT 2-input shared
6-in LUT
6-in LUT + 6-in LUT 4-input shared

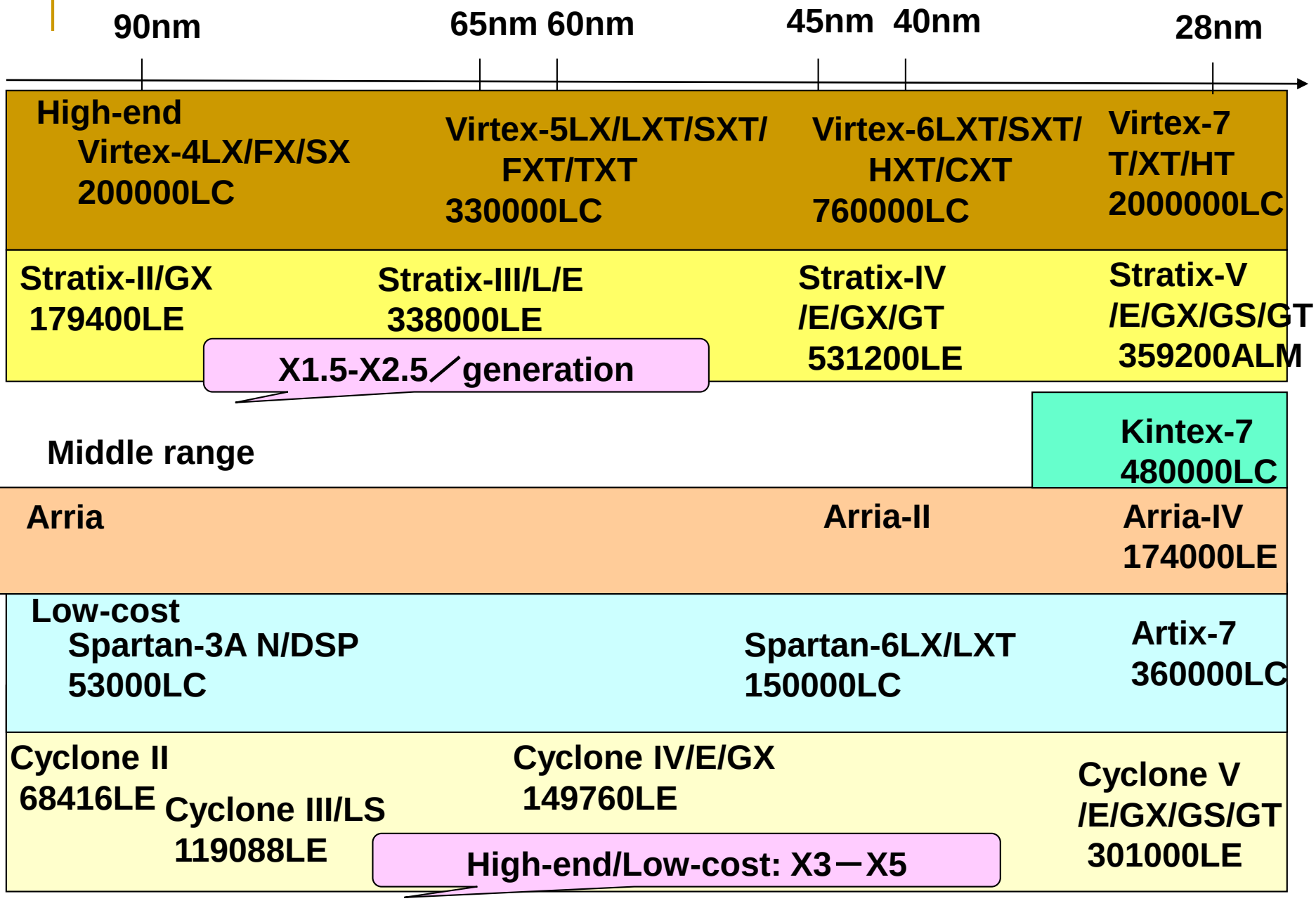
Stratix-IV manual

Stratix-IV LAB structure

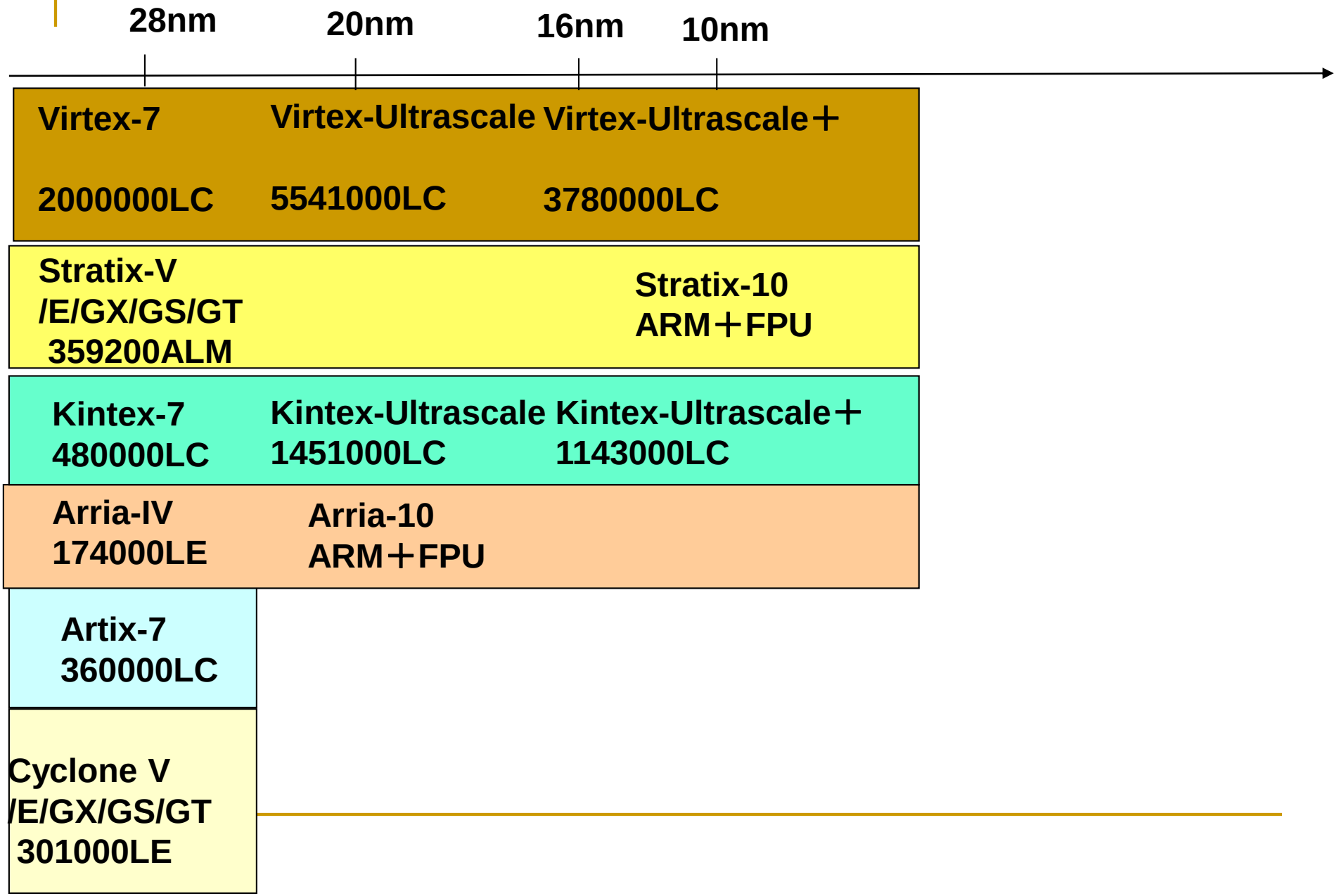


Stratix-IVマニュアルより

Technologies vs. Product



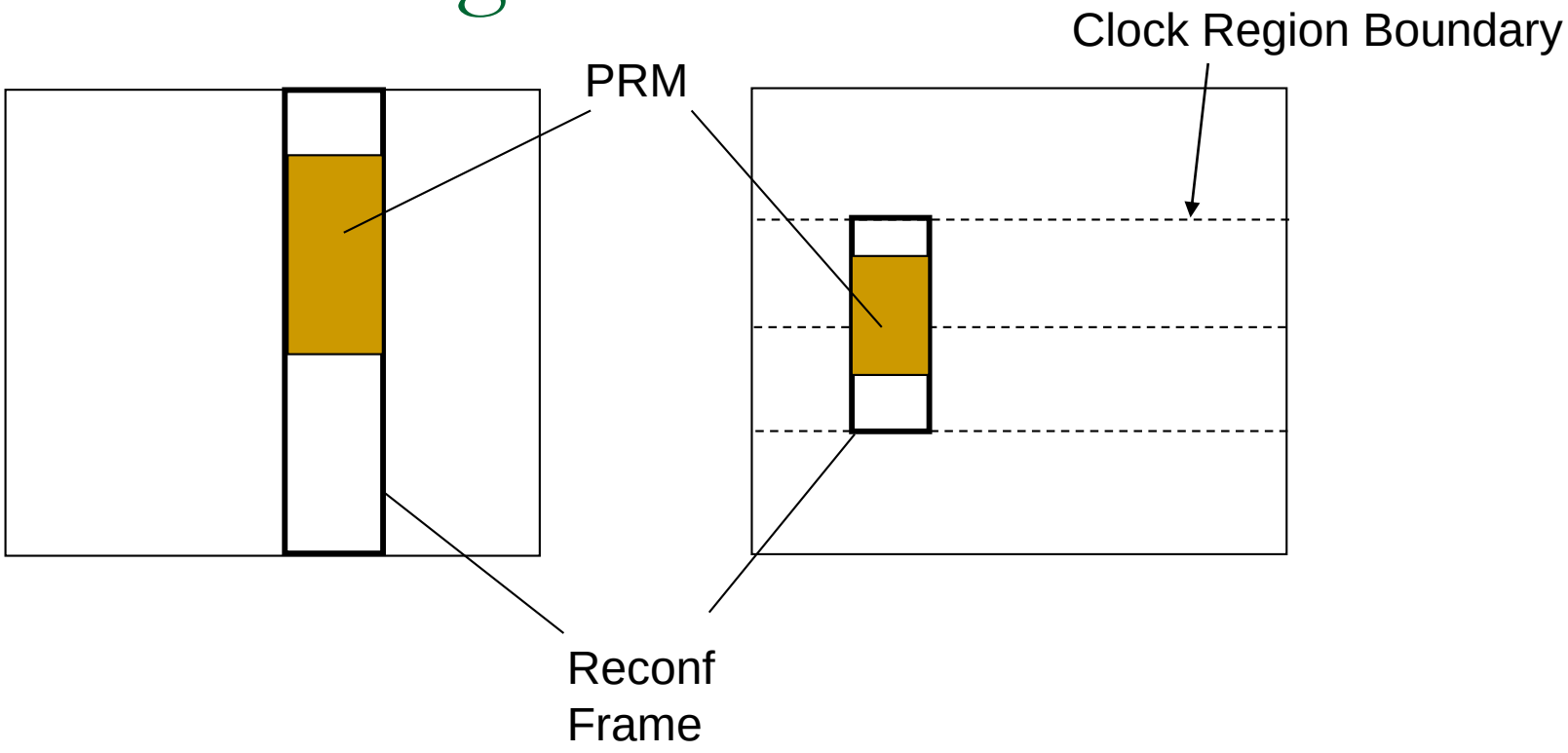
Technology vs. Products (Cont.)



Partial Reconfiguration

- A part of configuration on FPGA can be replaced during operation.
- Efficient use of FPGA area
  - Virtex-IIPro → Column by column
  - Virtex-4 → Rectangle shape
  - Virtex-6→ Dynamic Reconfiguration Port（DRP) is provided.
    - Partial reconfiguration is controlled by the logic in FPGA
  - Operating Systems for FPGA have been developed.

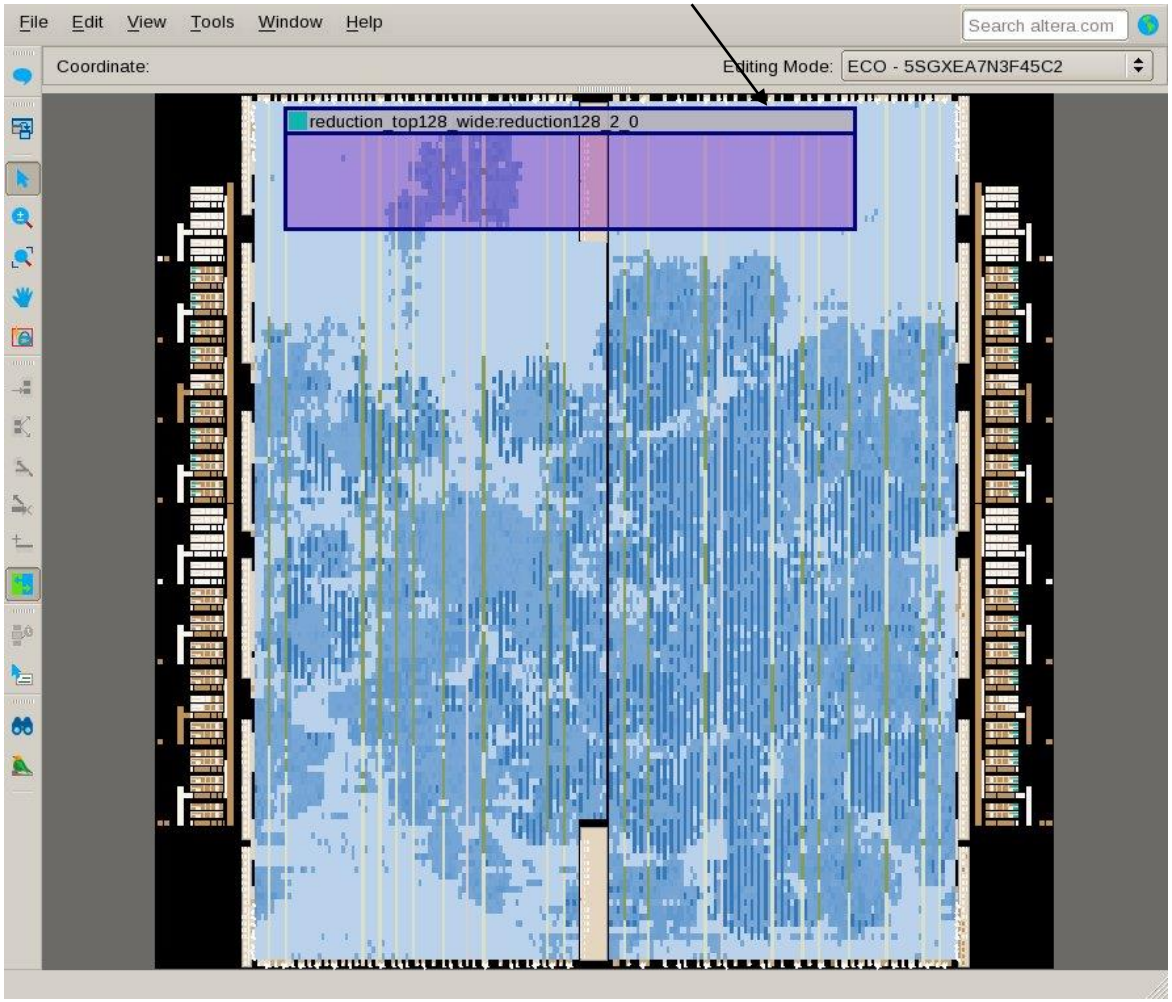
Partial Reconfiguration



PRM(Partial Reconfigurable Module) is placed on a fixed frame.

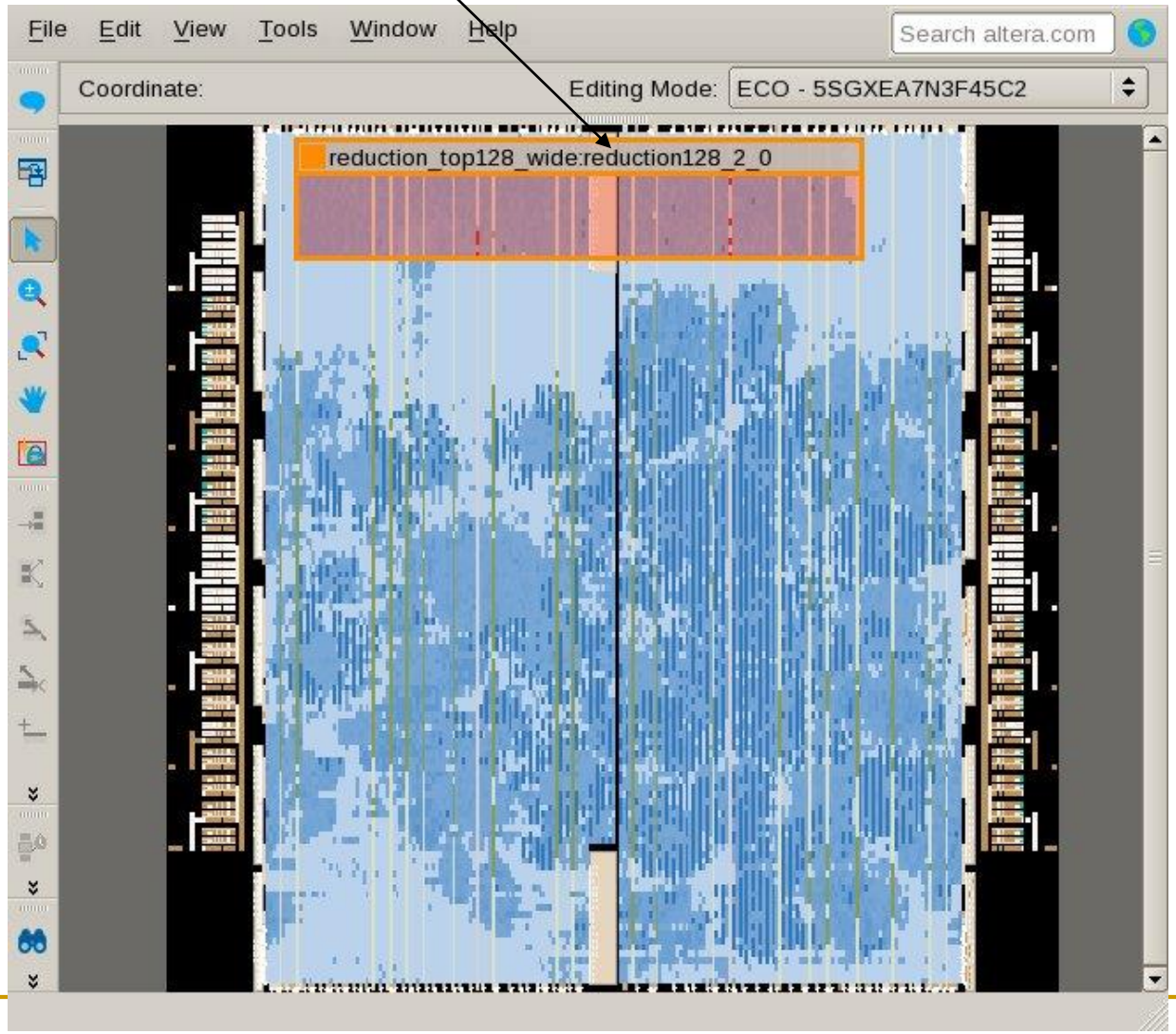
The problem is the interconnection between partial reconfiguration module and static part.

Partial Reconfiguration region



The case of Altera(Intel)’s Stratix V

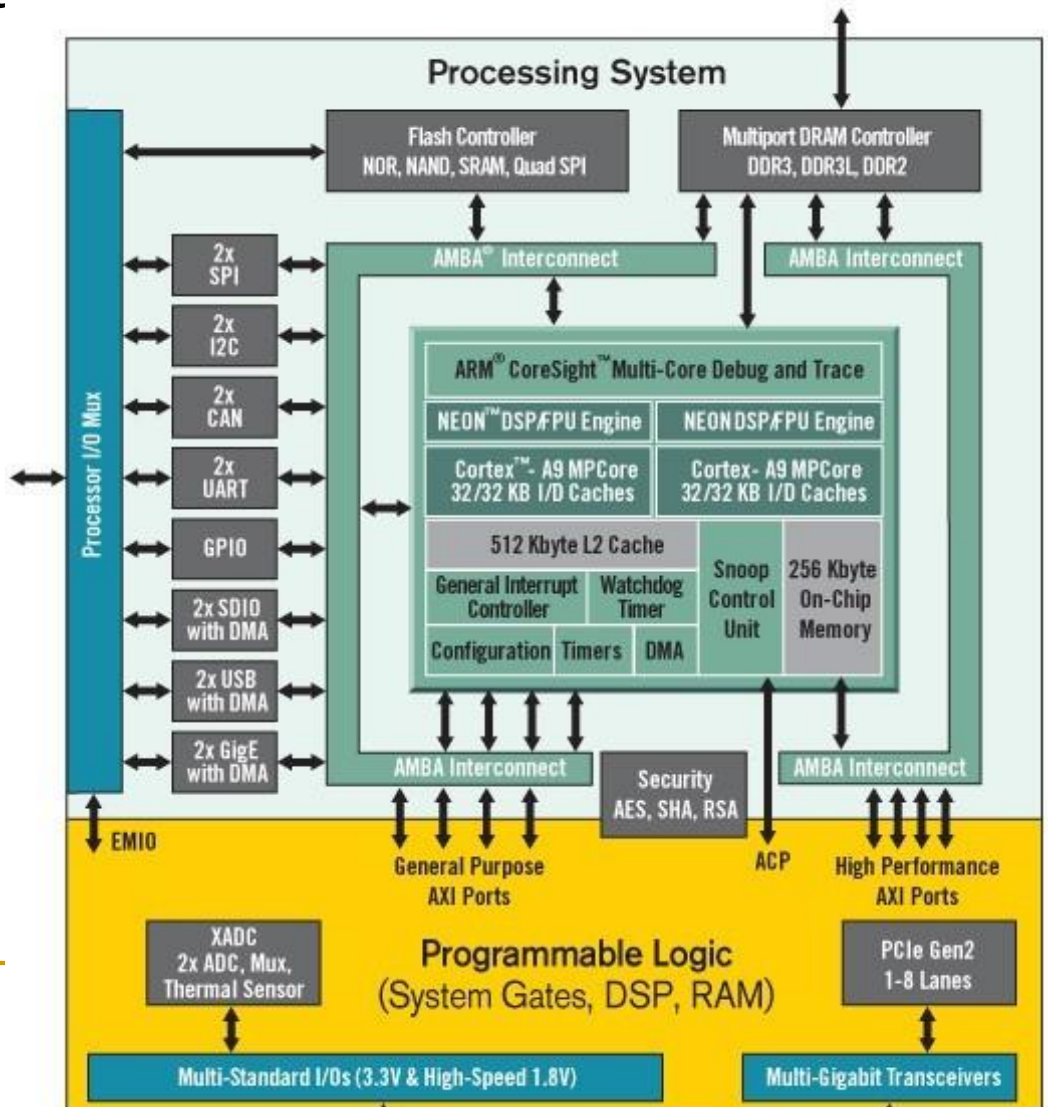
Replacing with another accelerator

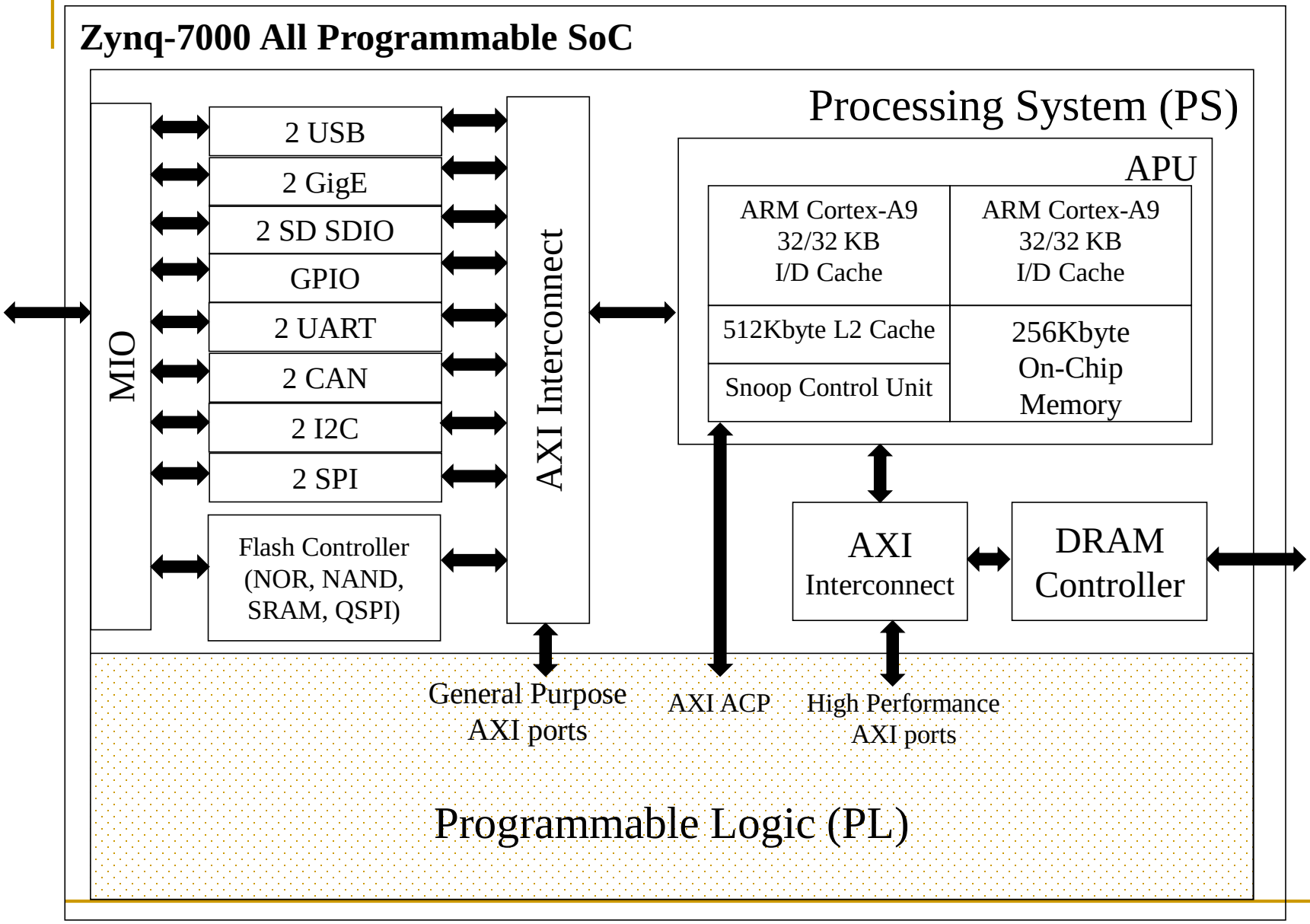


Main switching fabrics works without stopping.

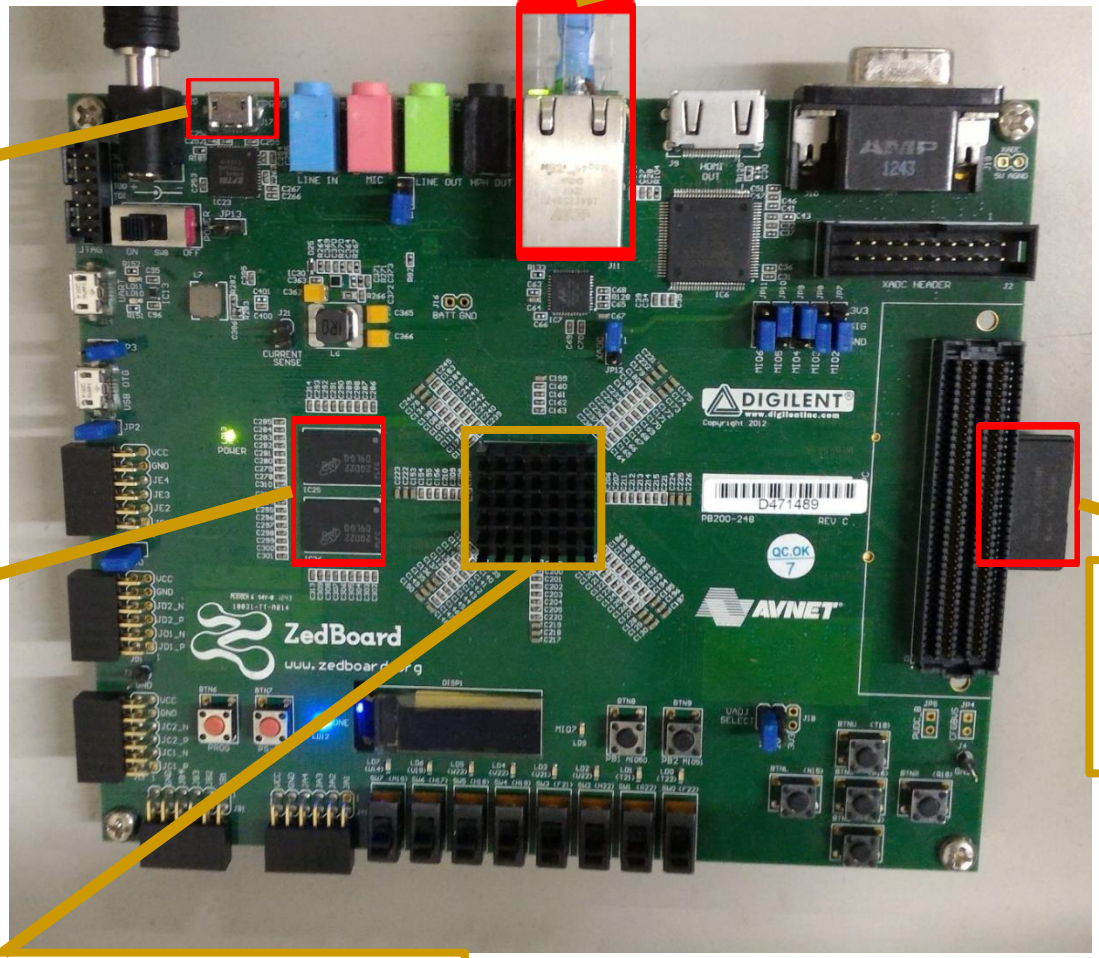
Zynq All programmable SoC

- ARM Cotex-A9（PS part) Dual Core CPU +
- 28nm Artix-7/Kintex-7 based FPGA（PL part)

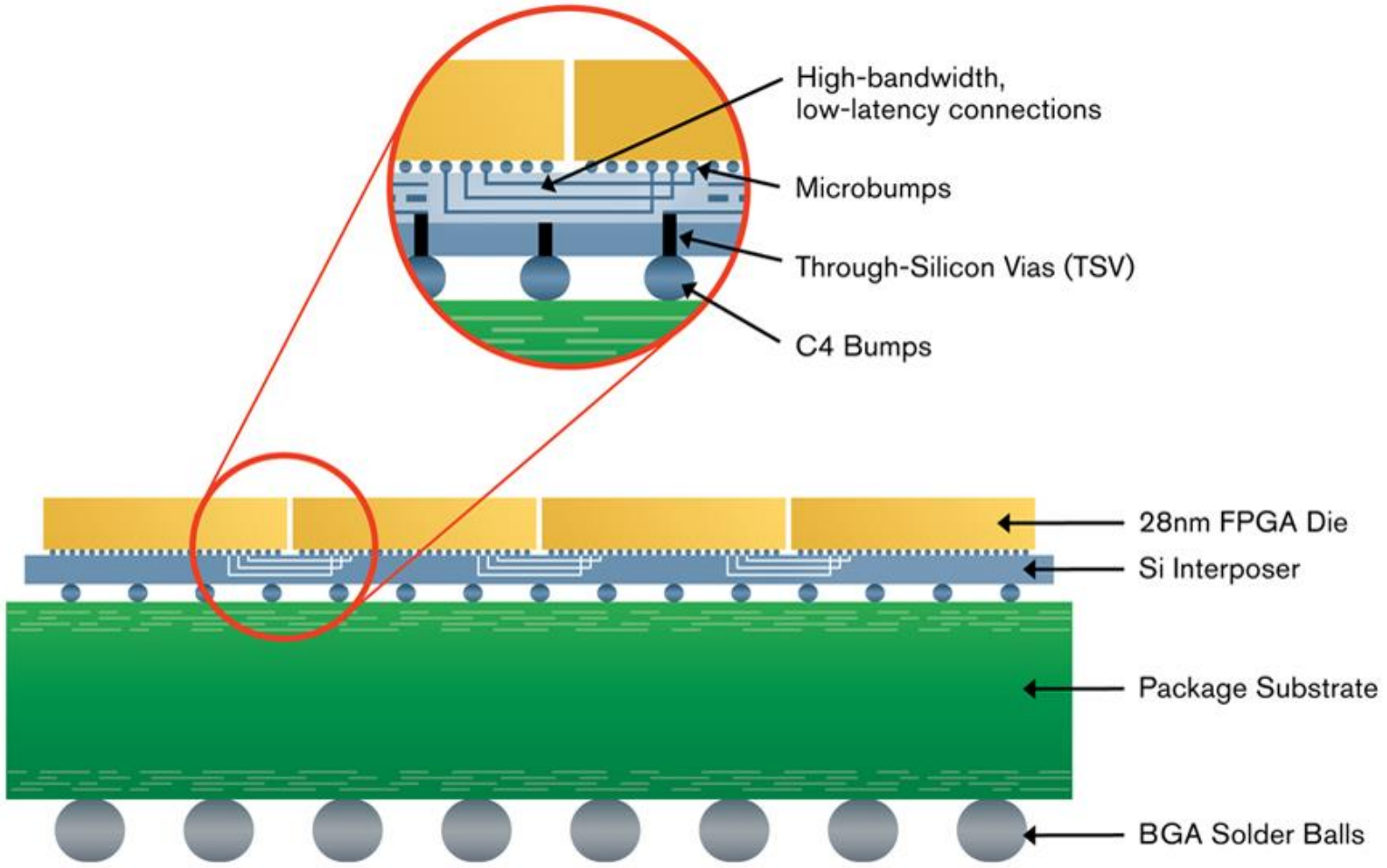



Zynq-7000 All Programmable SoC
Processing System (PS)
APU
ARM Cortex-A9
32/32 KB
I/D Cache
ARM Cortex-A9
32/32 KB
I/D Cache
512Kbyte L2 Cache
Snoop Control Unit
256Kbyte
On-Chip
Memory
MIO
2 USB
2 GigE
2 SD SDIO
GPIO
2 UART
2 CAN
2 I2C
2 SPI
Flash Controller
(NOR, NAND,
SRAM, QSPI)
AXI Interconnect
AXI
Interconnect
DRAM
Controller
General Purpose
AXI ports
AXI ACP
High Performance
AXI ports
Programmable Logic (PL)

dBoard

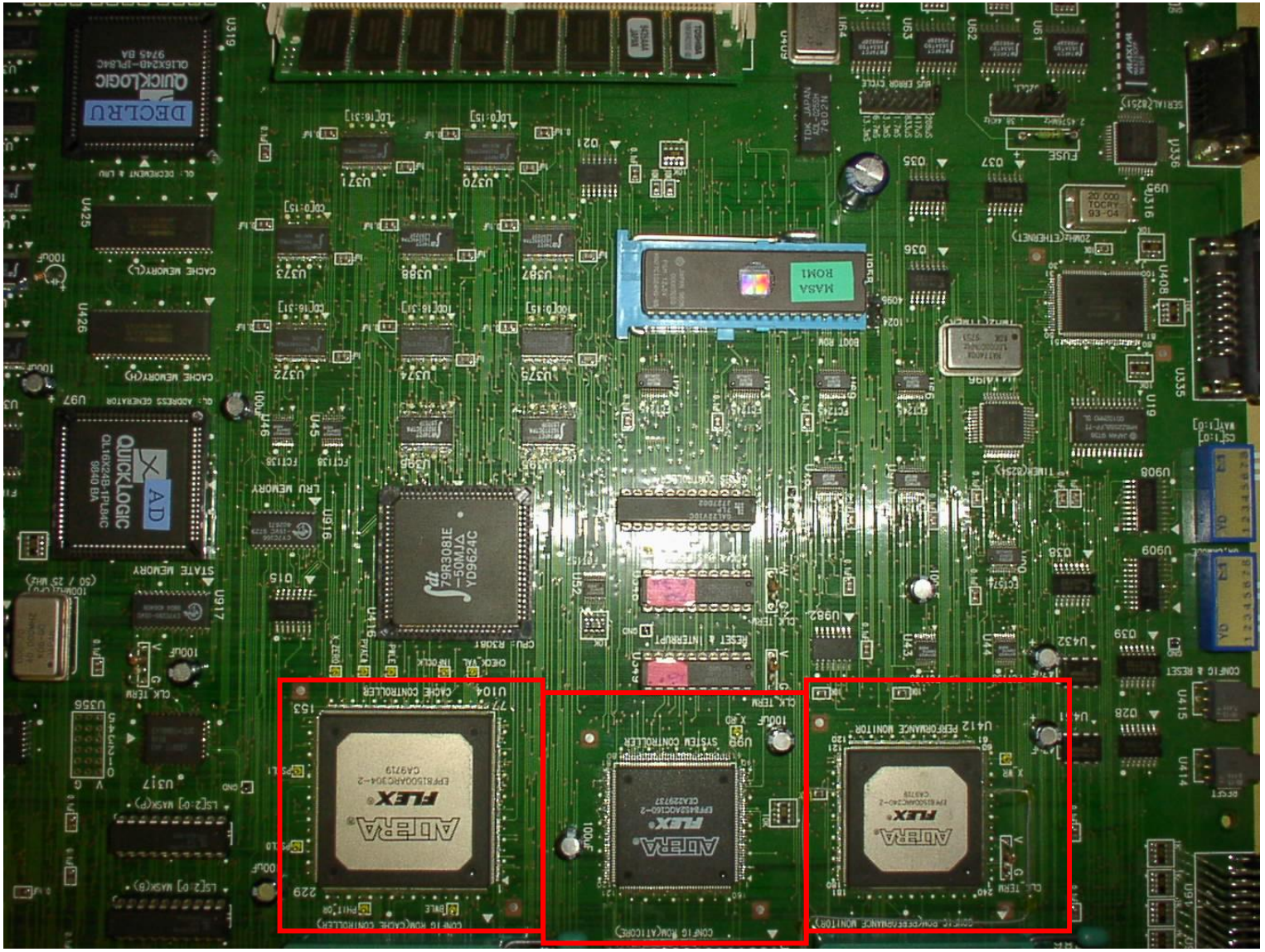

Ethernet
JTAG
DDR3 512MB
SD Card installed Linaro Ubuntu
Zynq-7000 All Programmable SoC XC7Z020-CLG484-1
ZedBoard
DIGILENT
AVNET

2.5D FPGA (http://www.xilix.com)

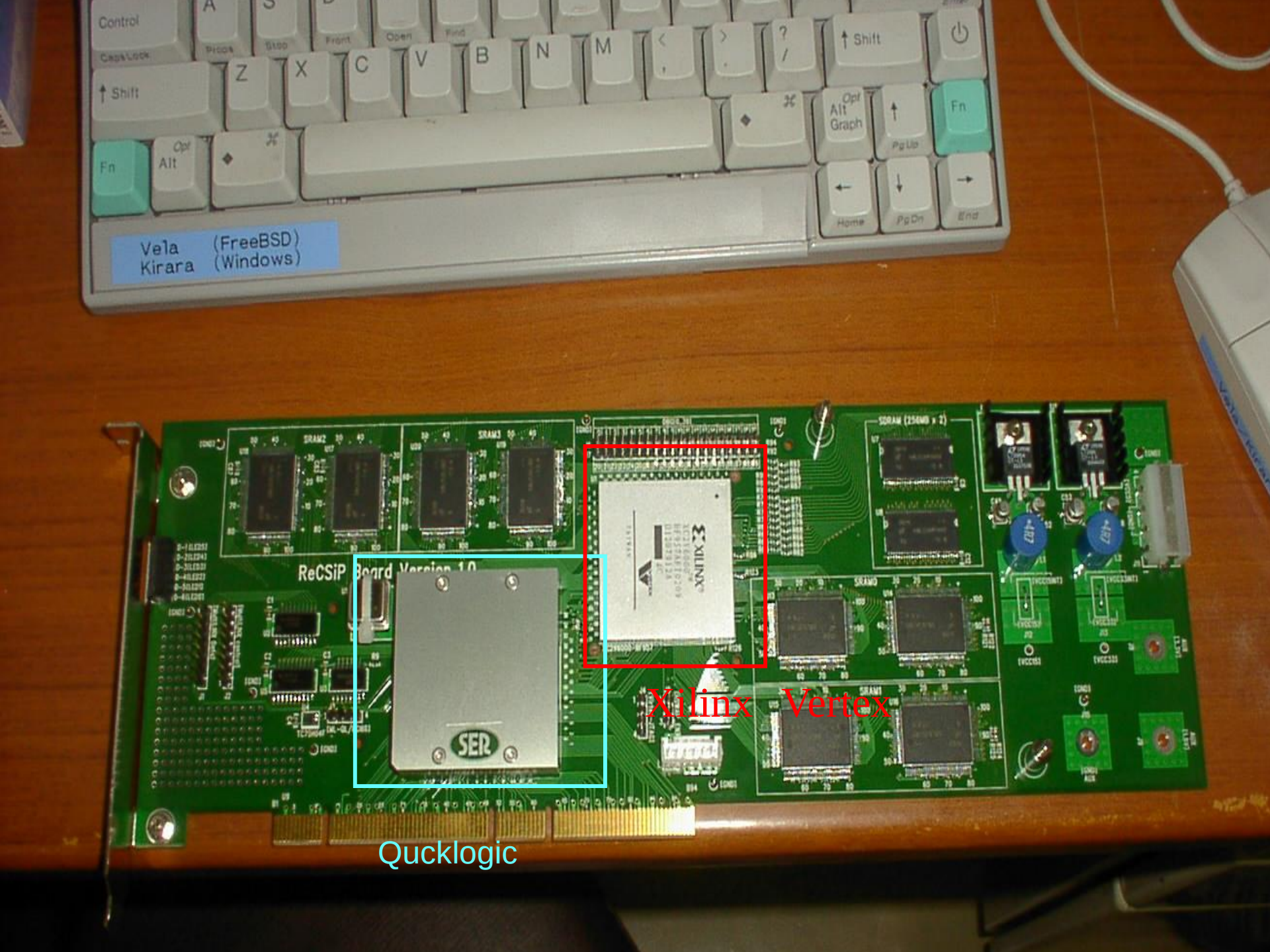


QuickLogic

Lattice GAL



Altera FLEX10K

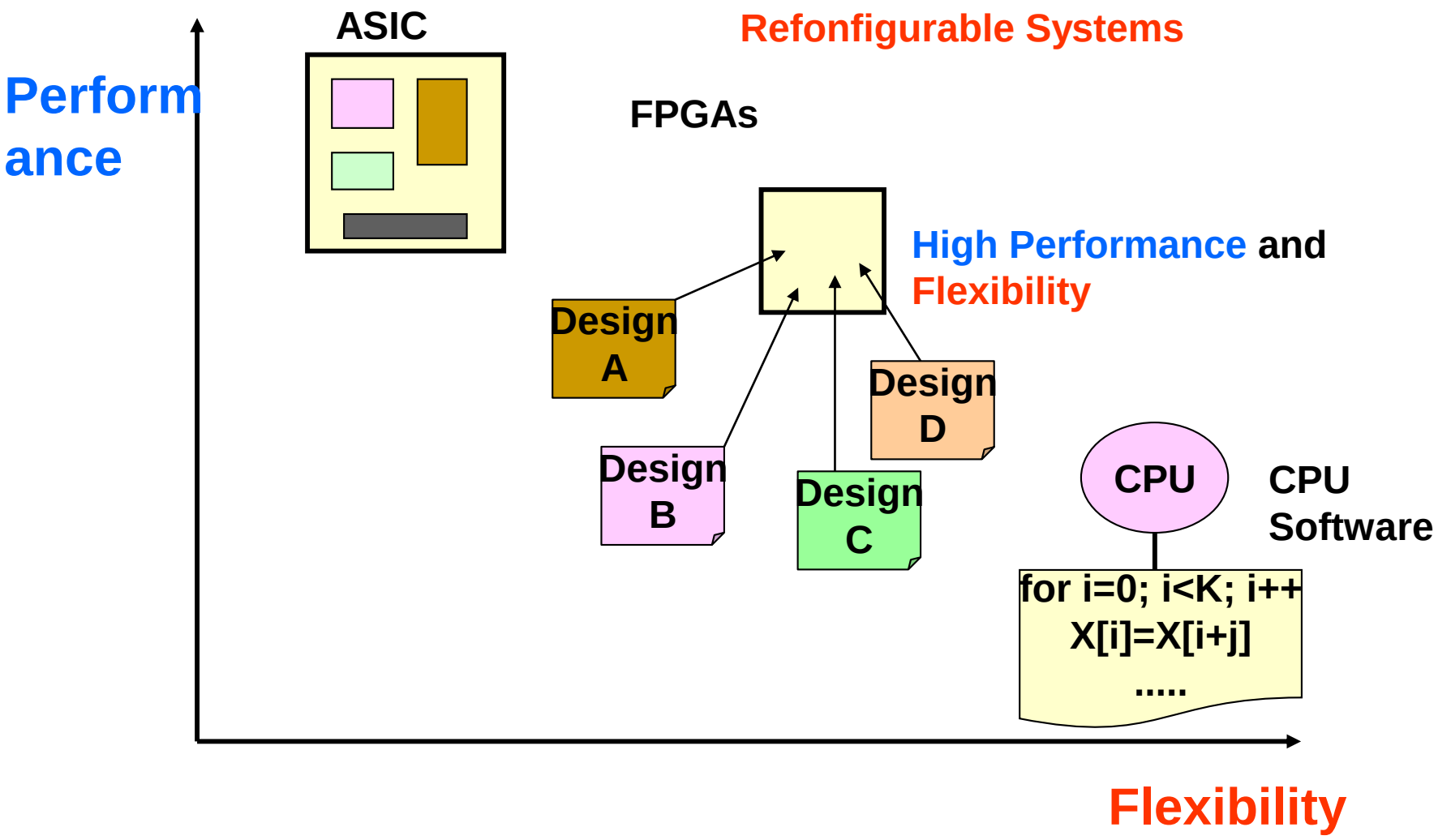

Vela (FreeBSD)
Kirara (Windows)
ReCSiP
Xilinx Vertex
Qucklogic

Design of PLDs

- Mostly designed with common HDL（Verilog-HDL, VHDL)
  - C level entry is used recently: Impulse-C, Vibado(Xilinx), Open-CL(Altera)
- Synthesis, optimization, place and route is automatically done by vendors' tools.
  - Integration and combination of tools from various venders are used recently.
  - For large circuit, a long time is required especially for place and route.
  - Using IPs, clock/DLL adjustment is manually done.
  - Optimization techniques are different from vendors/products.

Reconfigurable System (Custom Computing Machine)

- A target algorithm is executed directly with a hardware on SRAM-style FPGA/PLDs.
  - High performance of special purpose machines.
  - High degree of flexibility of general purpose machines.
- A completely different execution mechanism from a stored program computers.


Refonfigurable Systems
Performance
ASIC
FPGAs
High Performance and Flexibility
Design A
Design B
Design C
Design D
CPU
CPU Software
for i=0; i<K; i++
X[i]=X[i+j]
.....
Flexibility

How enhance the performance?

- Performance enhancement by hardware execution itself
  - The overhead of software execution (Instruction fetch, data load to registers, and etc.)
  - The overhead of using fixed size data.
  - The overhead of using only two way branches.

However, these benefits are not so large, for embedded CPU and DSP are highly optimized.

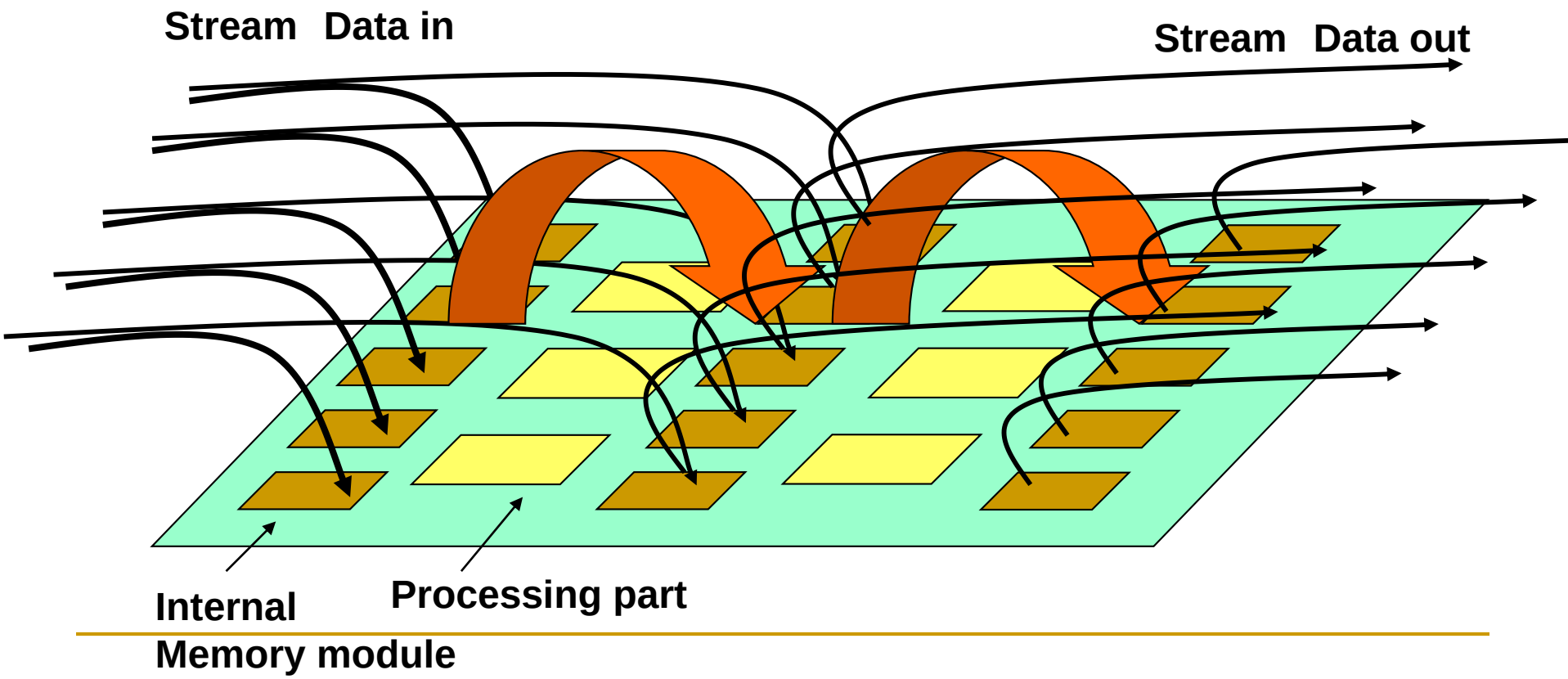
The key of performance improvement is parallel processing

Parallel processing in reconfigurable systems

- Various techniques can be used
  - SIMD execution
  - Pipelined structure
  - Systolic algorithm
  - Data driven control
- Parallel execution other than calculation
  - Parallel data access using internal memory units
  - Parallel data transfer including I/O accesses

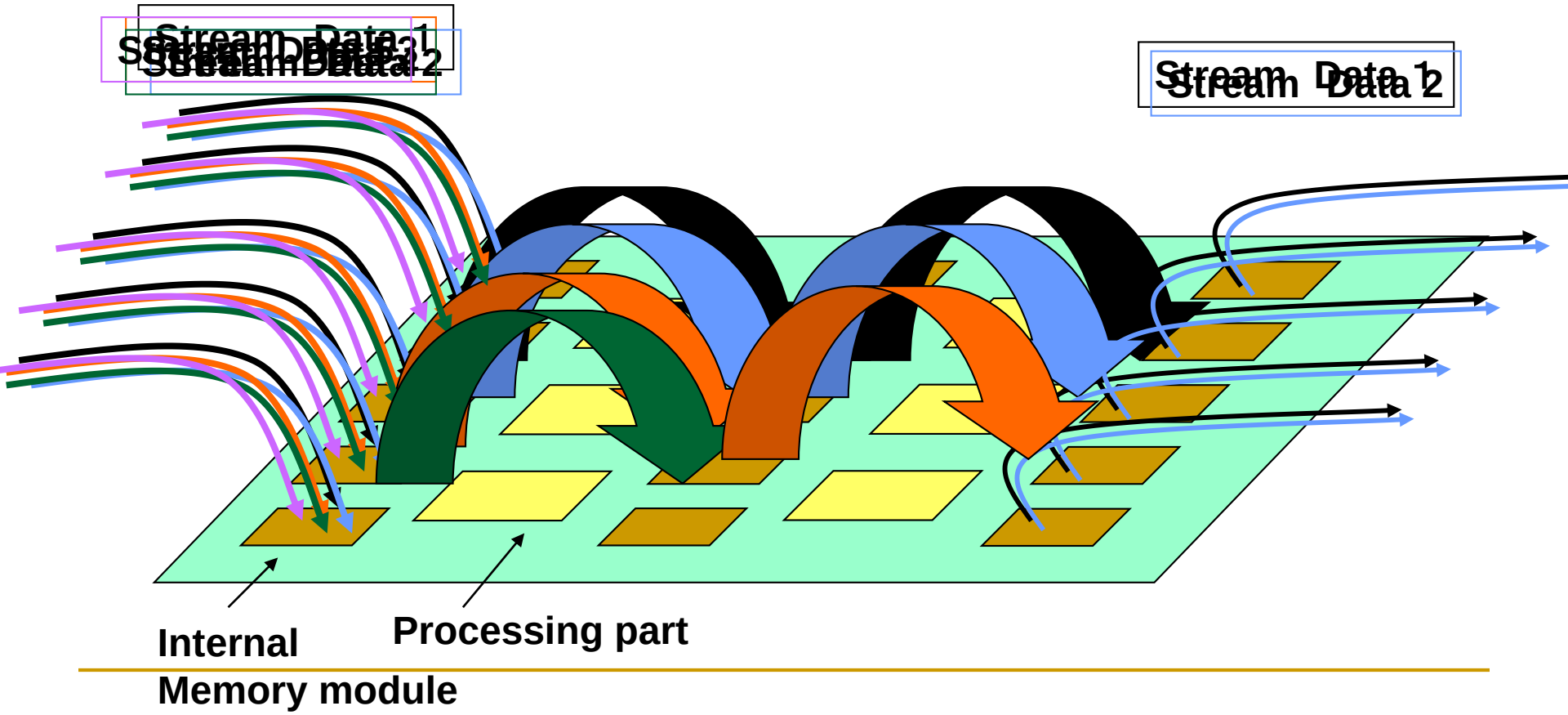
SIMD (Single Instruction-stream/ Multiple Data-stream)-like calculation

The same instruction is applied to different data stream
In Reconfigurable Systems, the operation is not required to be same
（SIMD-like calculation）

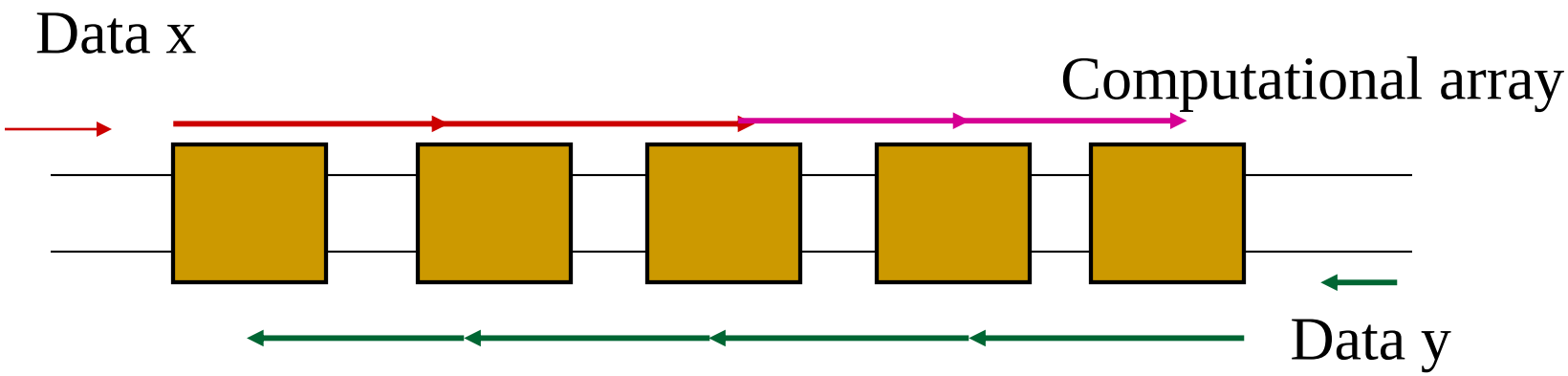


Pipelined structure

The stream is divided and inserted periodically.



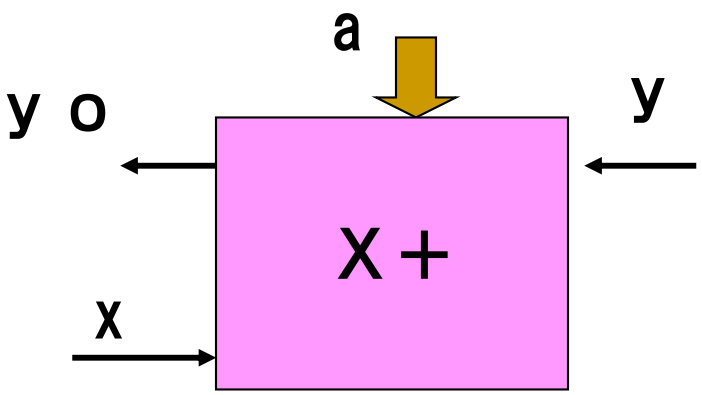
Systolic Algorithm



Data stream x, y are inserted with a certain interval.
When two stream meet each other, a calculation is executed.
→ Systolic: The beat of heart

Band matrix multiply y=Ax

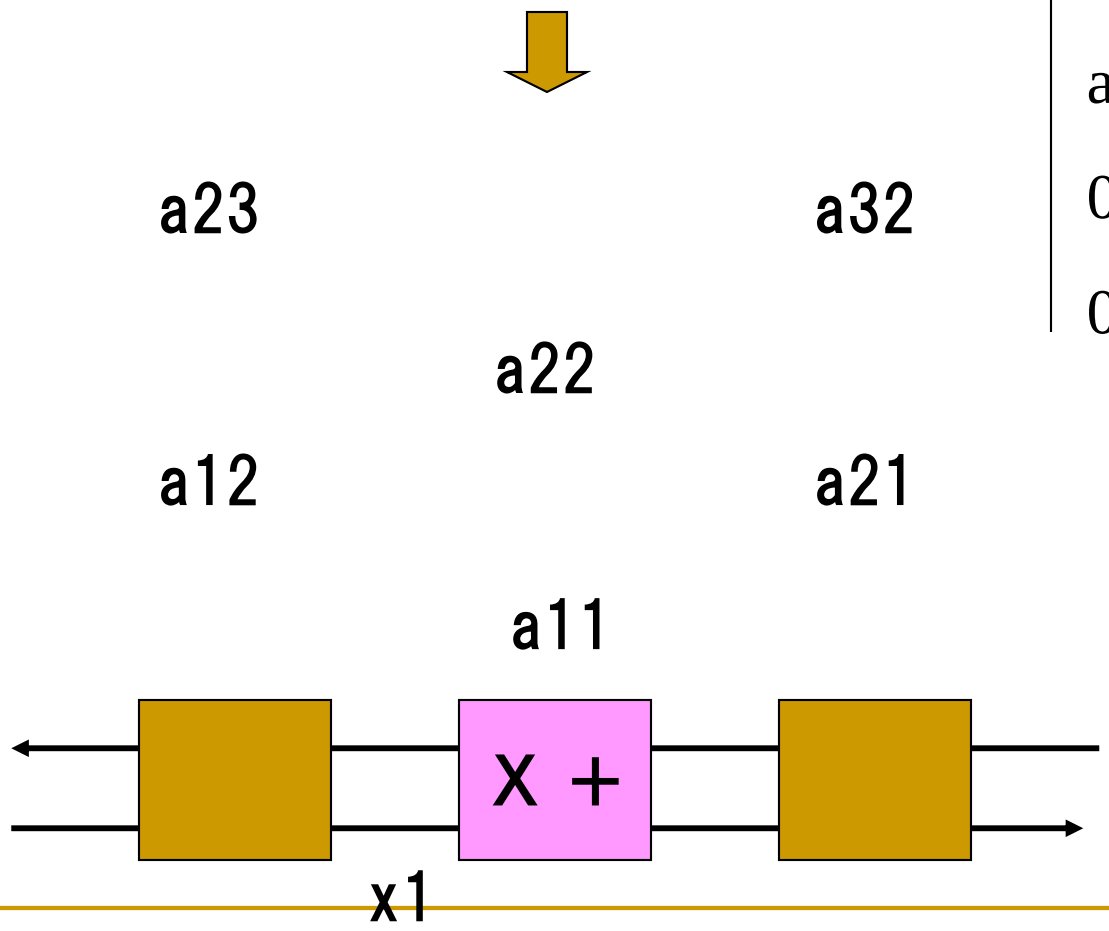
$$\begin{vmatrix} y0 \\ y1 \\ y2 \\ y3 \end{vmatrix} = \begin{vmatrix} a11 & a12 & 0 & 0 \\ a21 & a22 & a23 & 0 \\ 0 & a32 & a33 & a34 \\ 0 & 0 & a43 & a44 \end{vmatrix} \begin{vmatrix} x0 \\ x1 \\ x2 \\ x3 \end{vmatrix}$$



y o = a x + y i

Band matrix multiply y=Ax

$$\begin{vmatrix} a11 & a12 & 0 & 0 \\ a21 & a22 & a23 & 0 \\ 0 & a32 & a33 & a34 \\ 0 & 0 & a43 & a44 \end{vmatrix}$$



Band matrix multiply y=Ax

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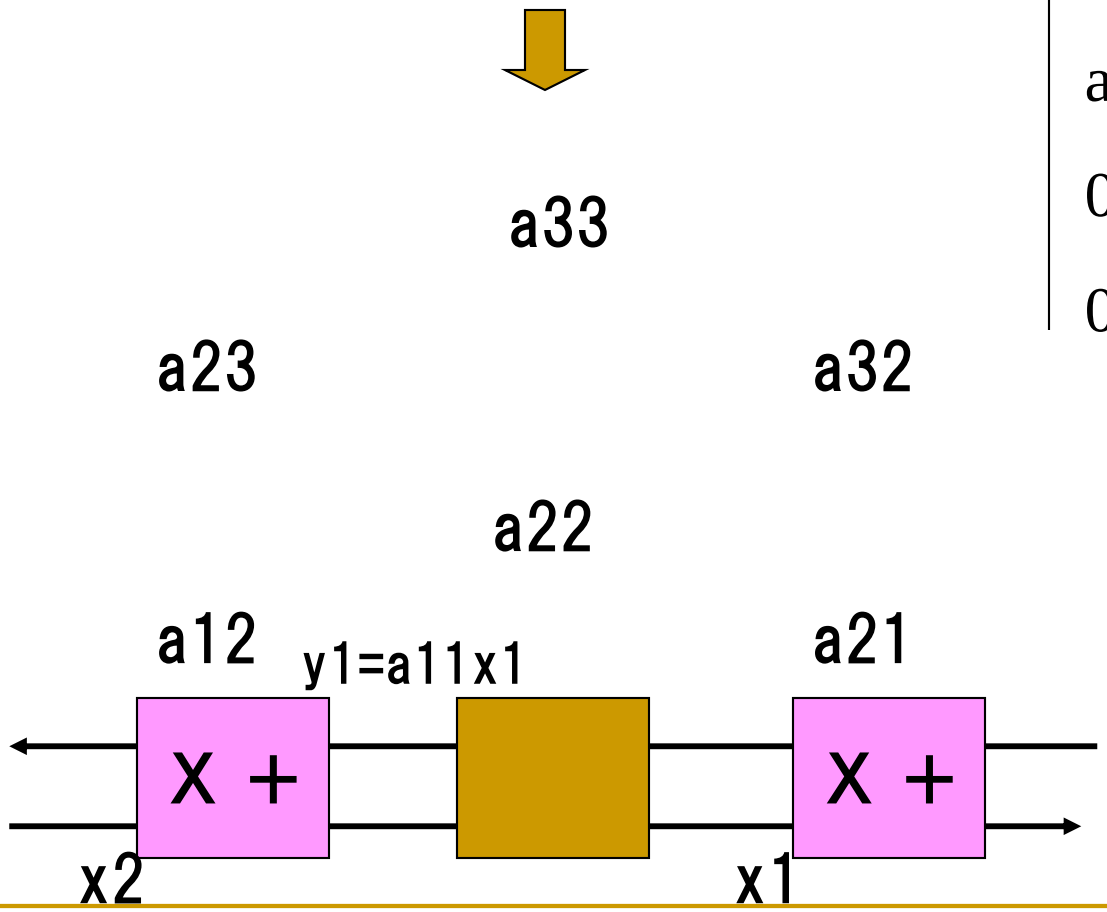

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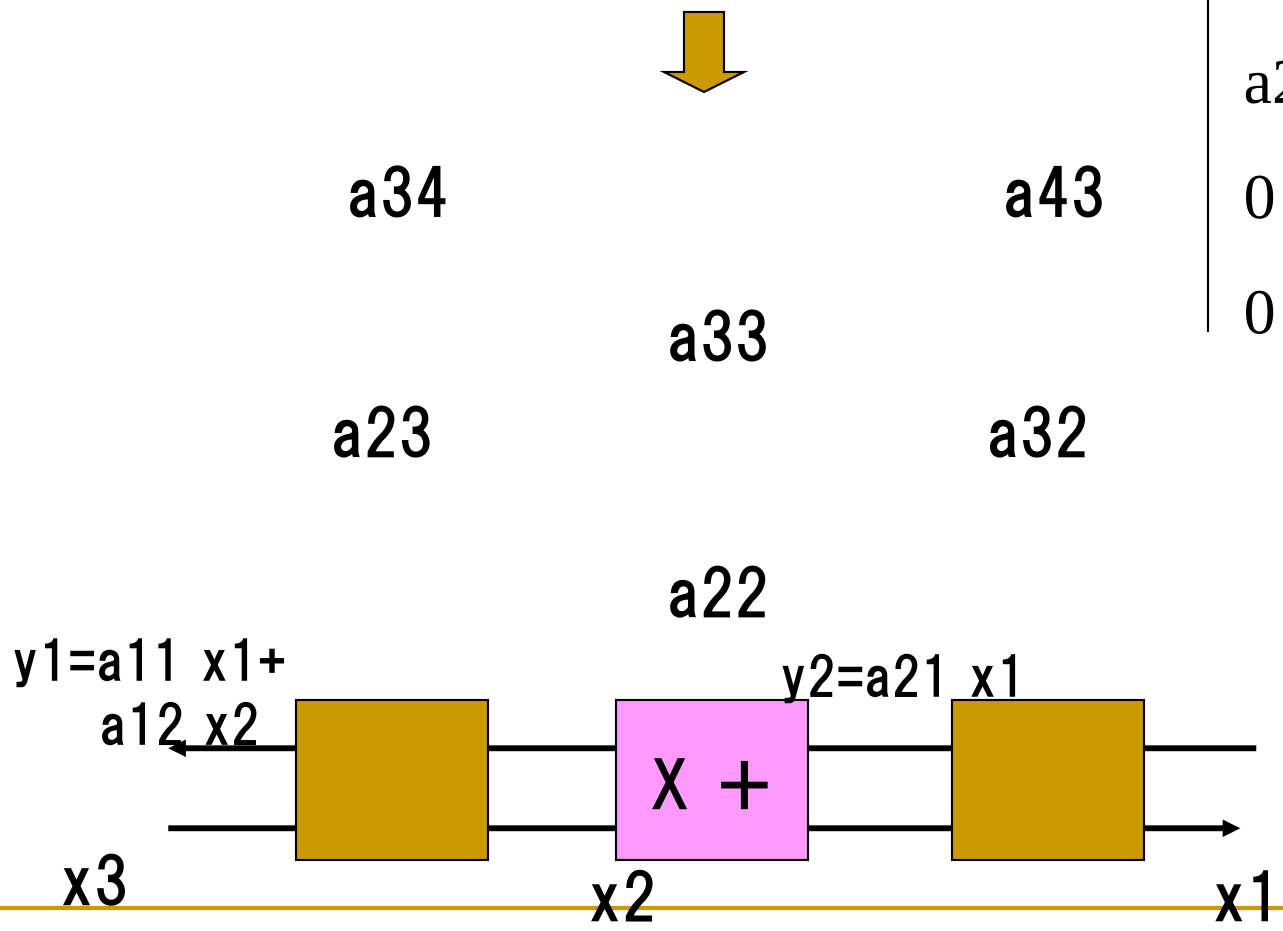

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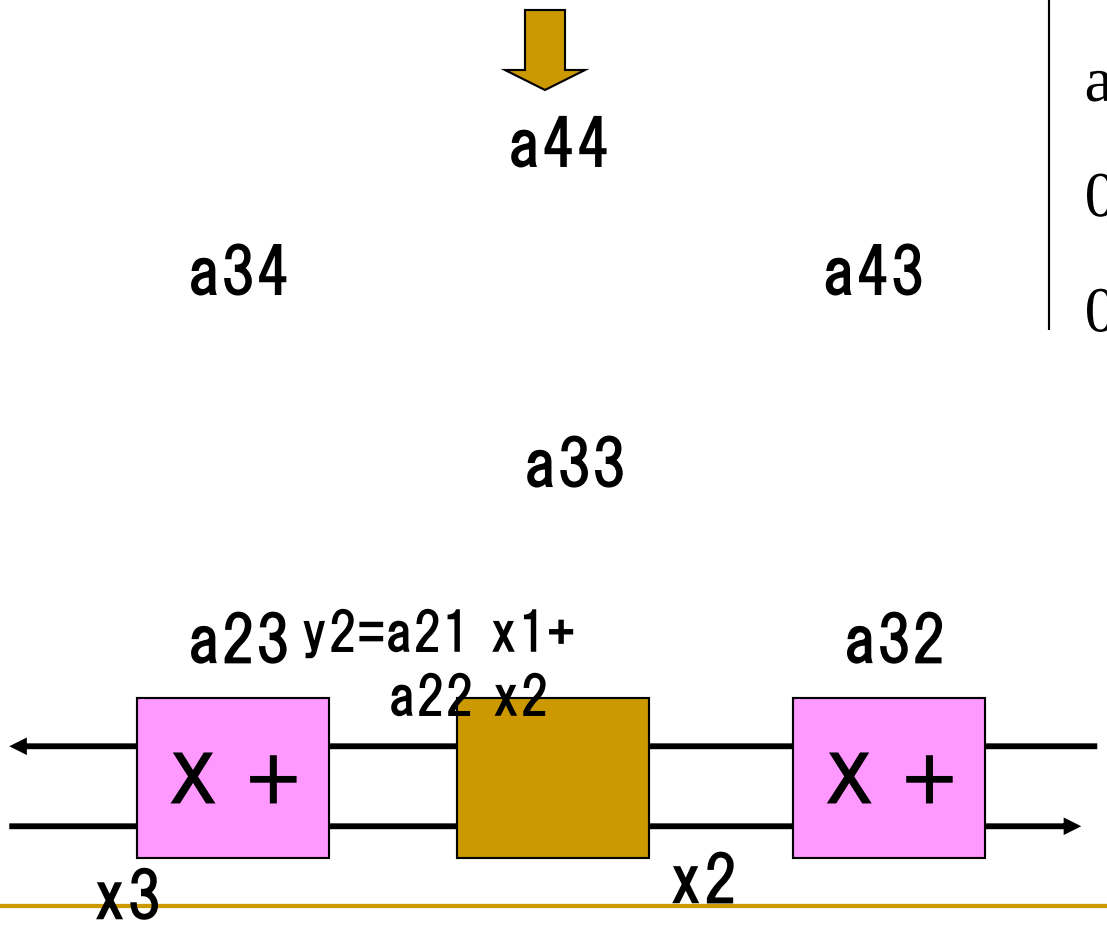
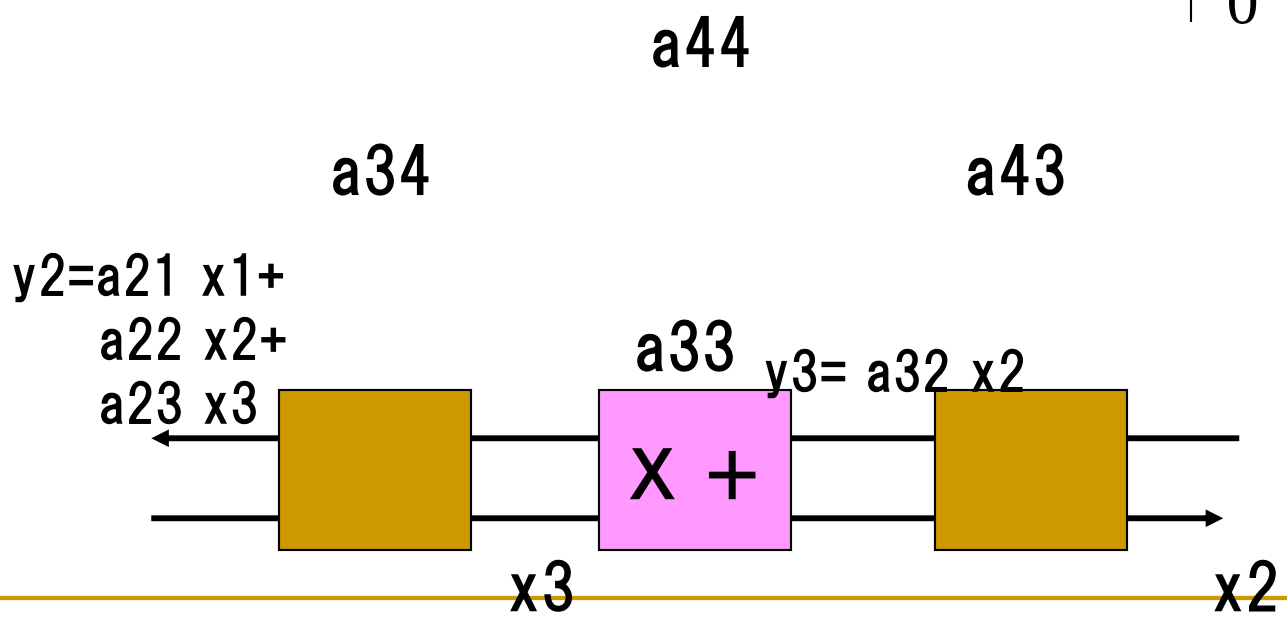
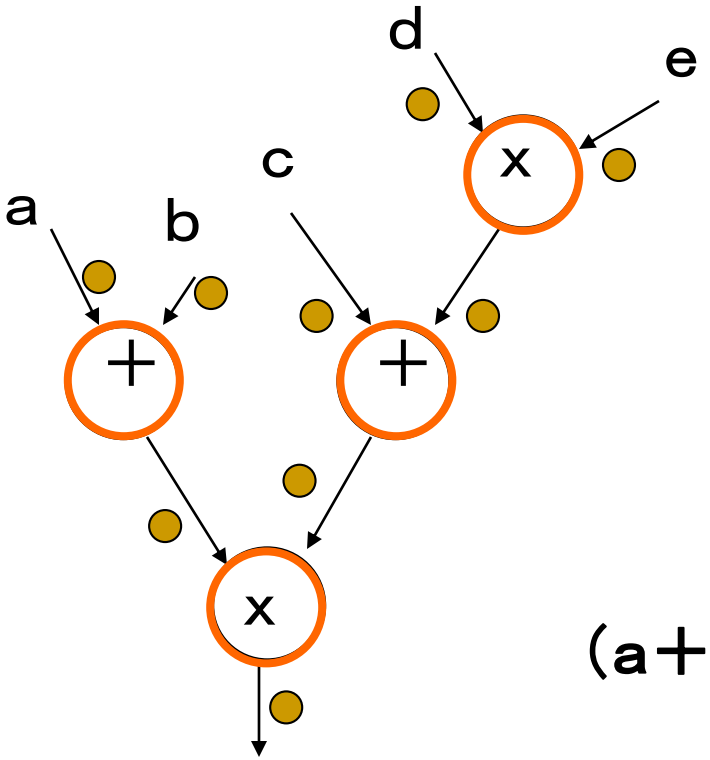


Band matrix multiply y=Ax

$$\begin{vmatrix} a11 & a12 & 0 & 0 \\ a21 & a22 & a23 & 0 \\ 0 & a32 & a33 & a34 \\ 0 & 0 & a43 & a44 \end{vmatrix}$$



Data flow algorithm



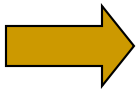
The process is activated with the available of tokens (data)

(a+b)x(c+(dxe))

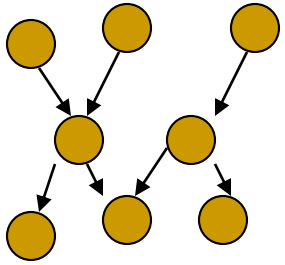
The overhead of synchronization is large.

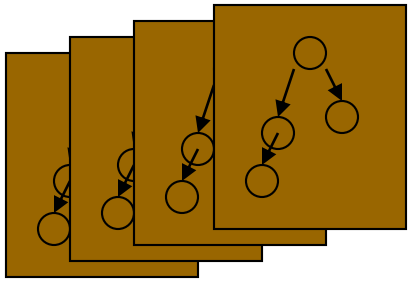
Data flow analysis and hardware generation

Data Flow Language



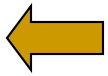
Data Flow Graph





Graph Decomposition

HDL Description



Configuration Data

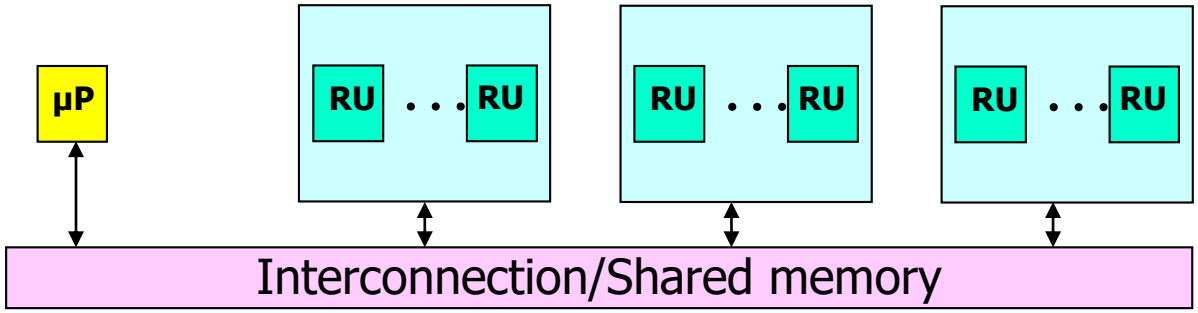
Suitable for automatic generation of hardware

Applications

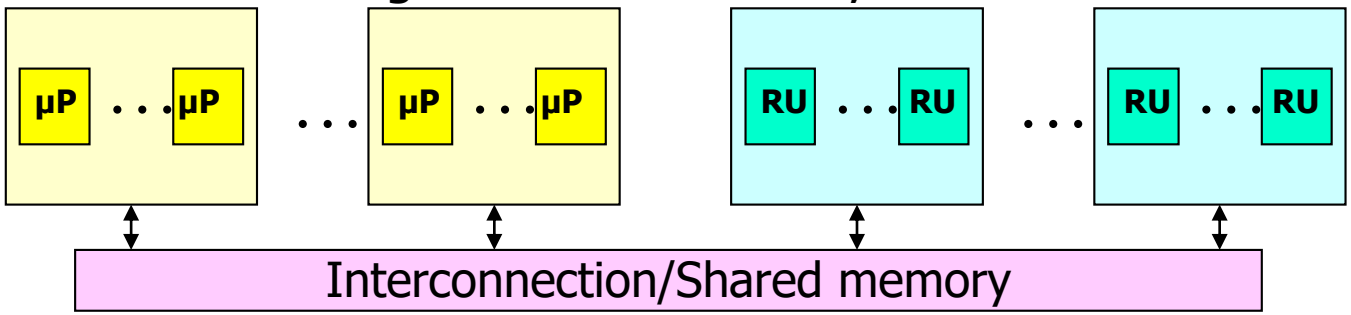
- No flexible program change
- No IEEE standard floating point
- Not memory bounded
  - Image processing, analysis, pattern matching,
  - Logic simulation, Fault simulation.
  - Neural network simulation.
  - Encryption /Decryption
  - Queuing Model、Markov Analysis
  - Electric Power Flow
  - Censer processing
- Efficient use of on the fly processing.
  - Communication control、Protocol control
  - Software radio

Large Scale Reconfigurable Platforms

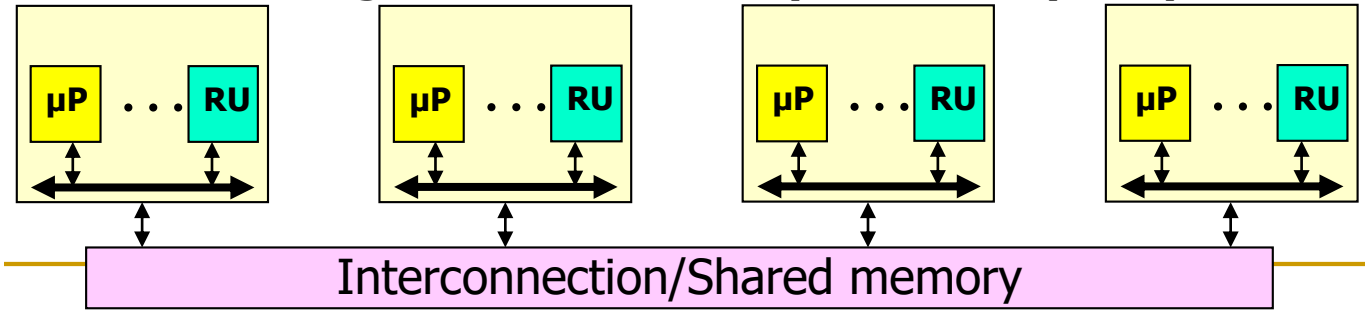
Stand-alone: **SPLASH, RASH,BEE2**



Hetero nodes using homo cores: **SRC6, SGI RASC**

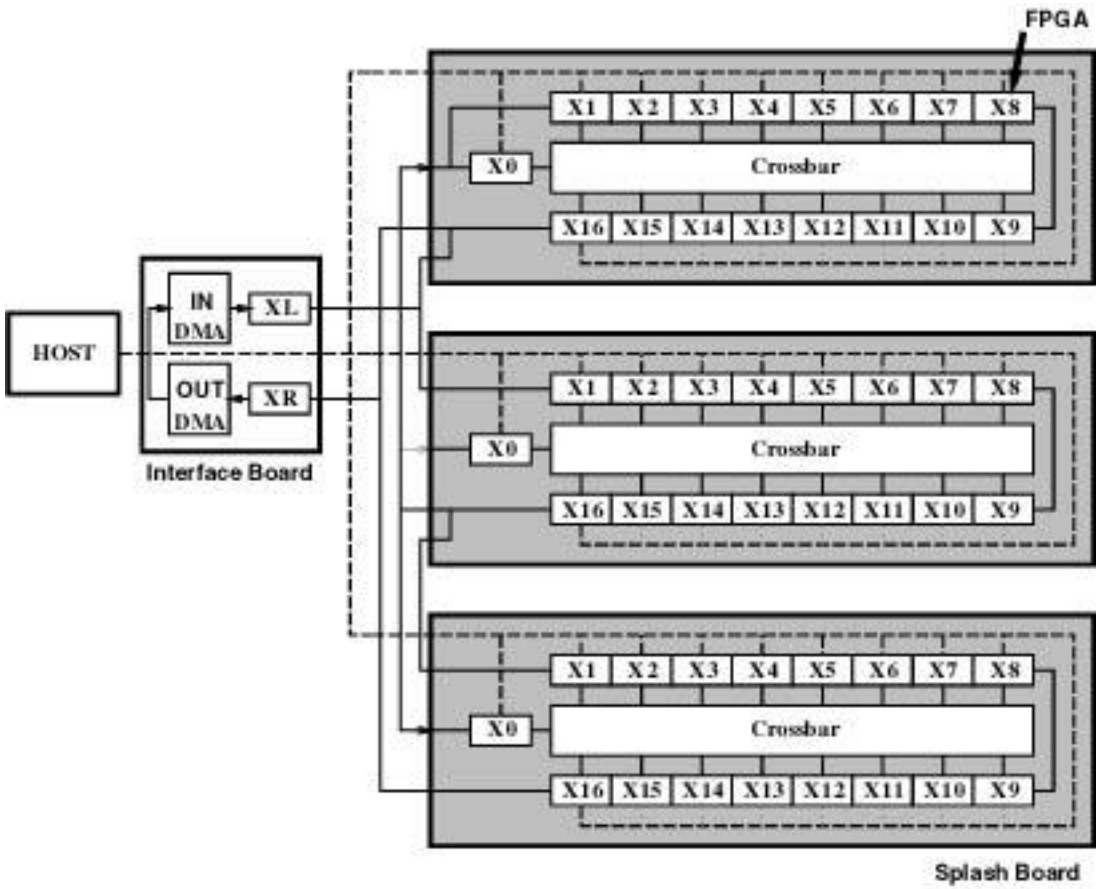


Homo node using hetero cores: **Cray XD-1, XT4(XR-1)**



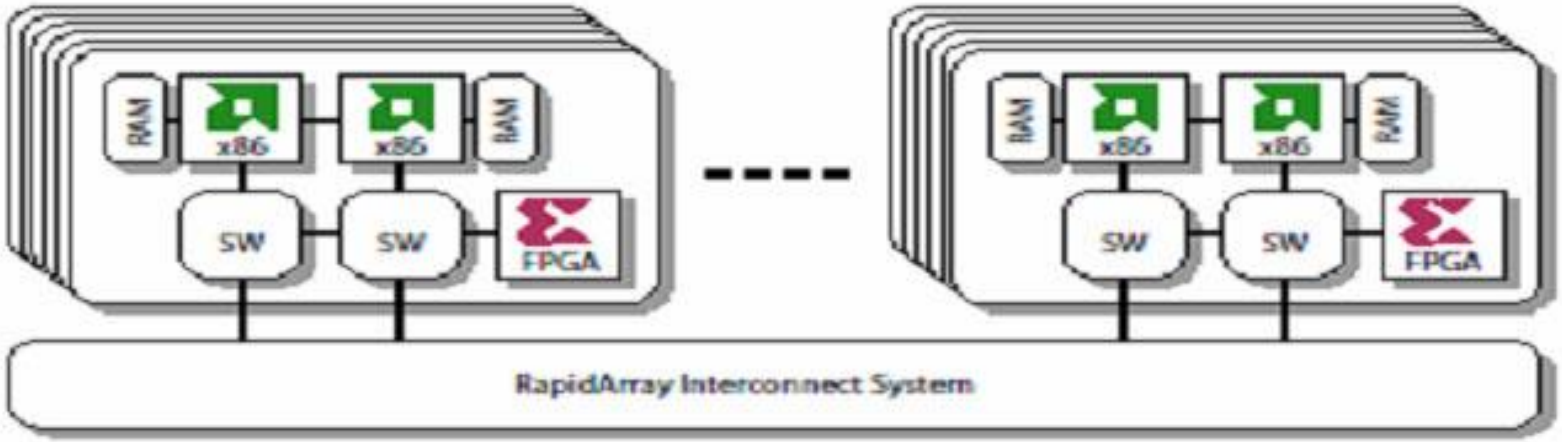
Splash-2 (Arnold et.al 92)

- String matching, Image processing, DNA matching, 330 times faster than the supercomputer Cray-II.
- Systolic algorithm
- VHDL, Parallel C
- Annapolis Micro Systems（WILDFIRE)



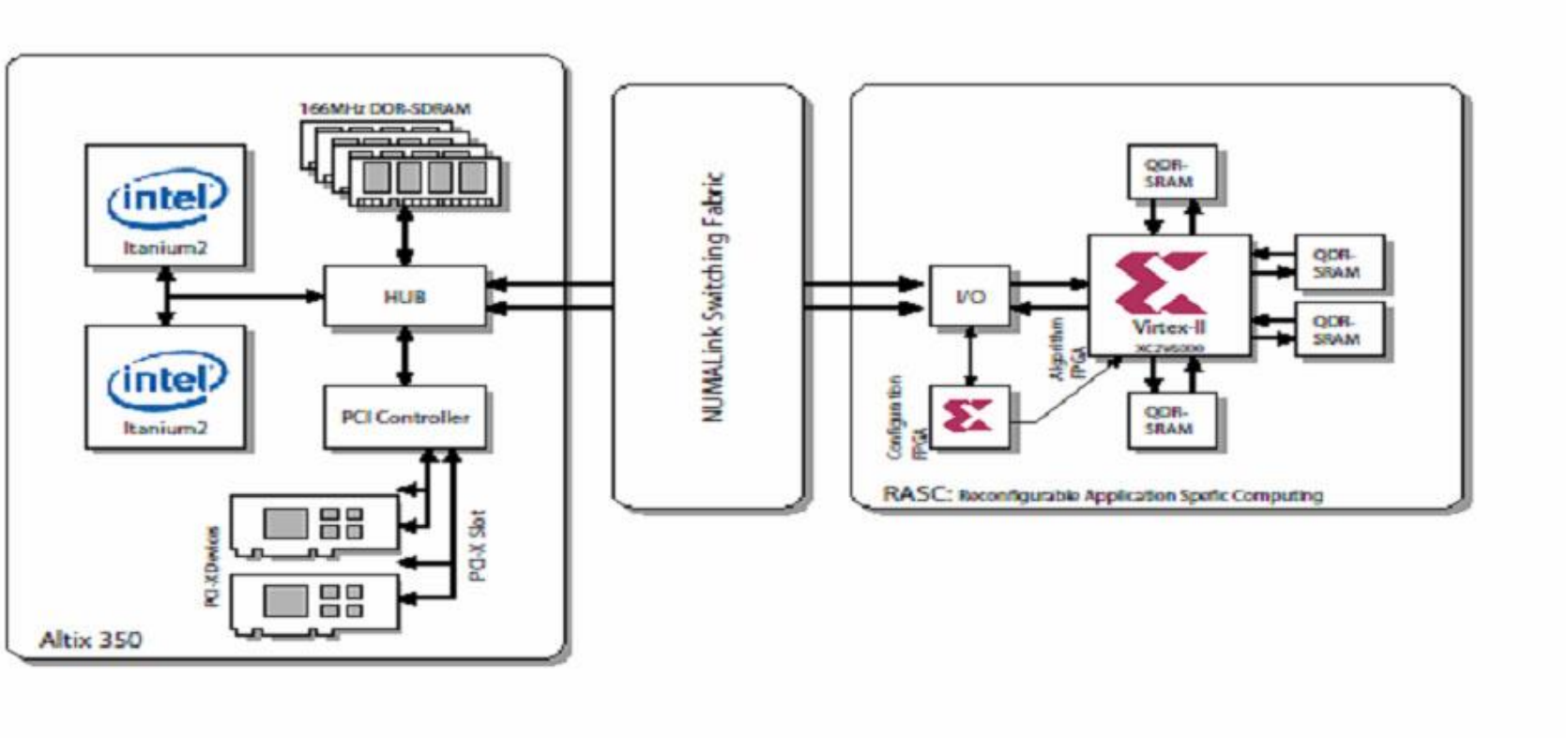
CRAY-XD1：

- AMD　Opteron
- 1board is consisting of 2CPUs＋FPGA（Virtex II Pro)
- 1 rack provides 6 boards
- A high speed network called Rapid　Array is used
- Interconnection between FPGAs can be done with Rocket I/O



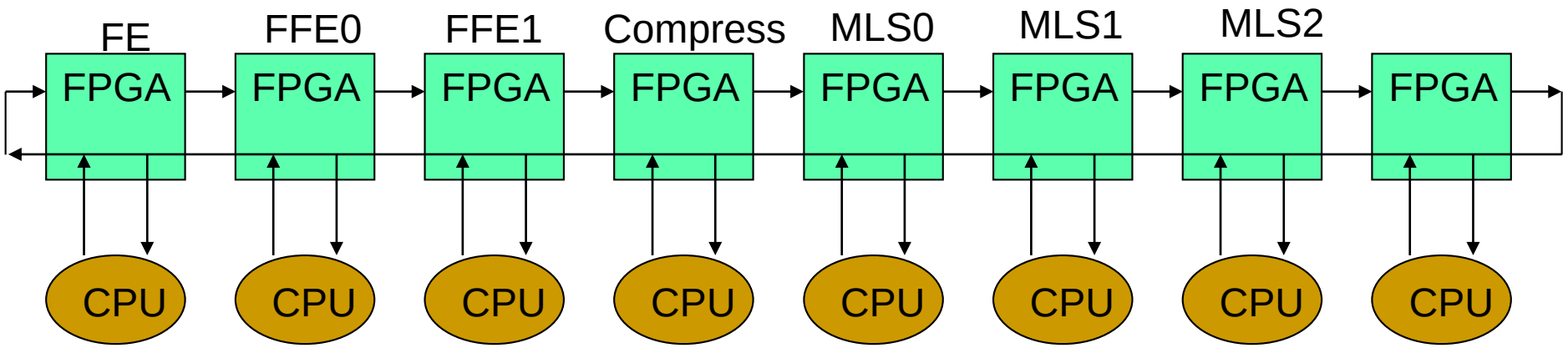
SGI RASC

- Accelerator for SGI's NUMA Altix
- Virtex II XC2V6000 and another Virtex for control
- Directly connected into the controller with NUMAlink4



Microsoft's Catapult

Rank computation for Web search on Bing.
Task Level Macro-Pipelining (MISD)
FE: Feature Extraction
FFE: Free Form Expression: Synthesis of feature values
MLS: Machine Learning Scoring



FPGA: Altera's Stratix V

2-Dimensional Mesh is formed (8x6) for 1 cluster.

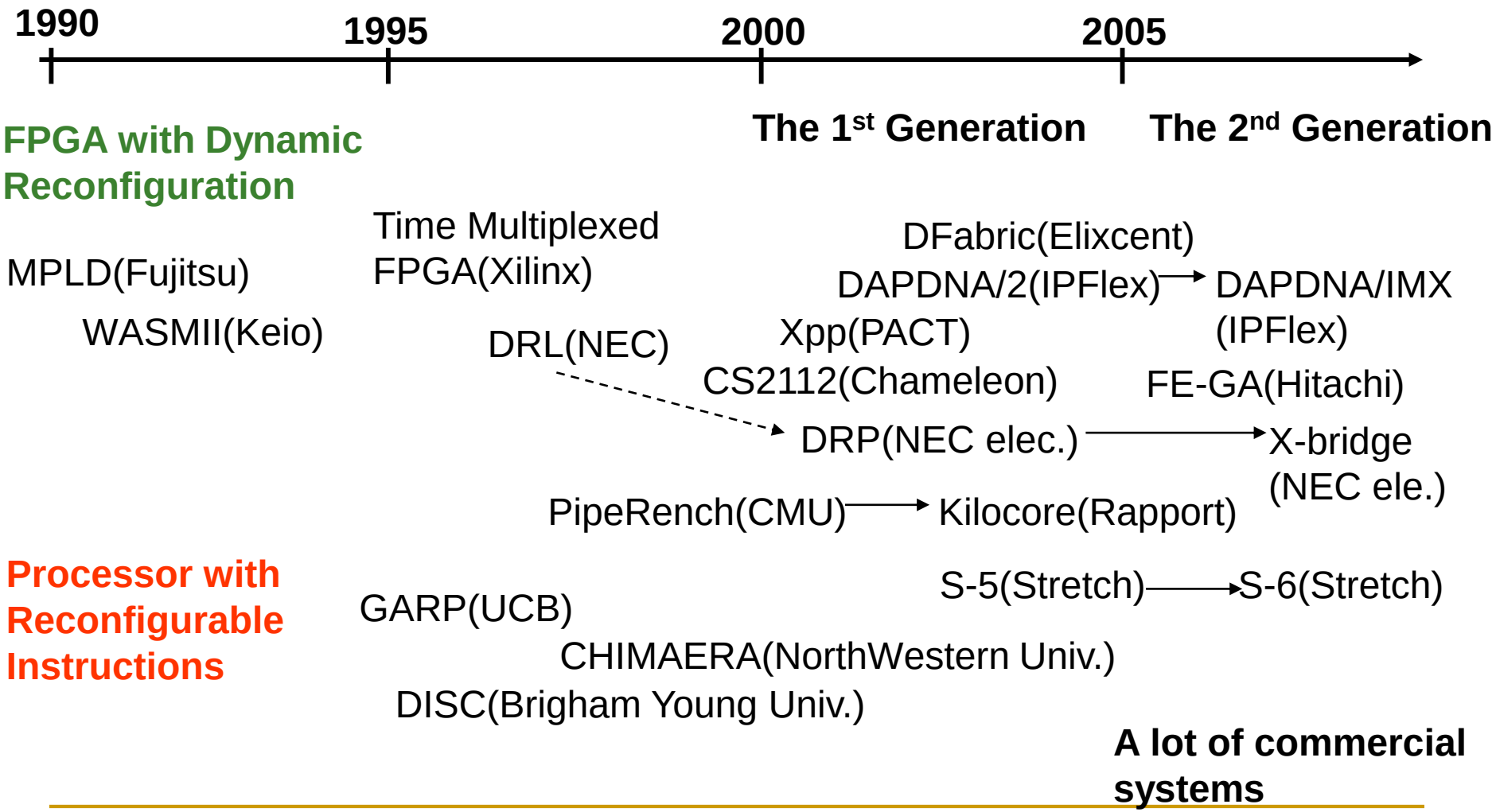
Recent trend of reconfigurable platforms

- Enough size of logic can be mounted on a single chip.
  - VL605 board (Virtex-6) or other boards can be a good platform of reconfigurable computing.
- A combination with embedded ARM core.
  - Zynq(Xilinx), Arria(Altera)
- Large platforms have been developed.
  - BEE3 Berkeley etc.
- Maxeler Technology's success on business.
  - Targets: Oil、Gas、Financial Analytics
  - Selling Solution using FPGAs

Dynamically Reconfigurable Processors

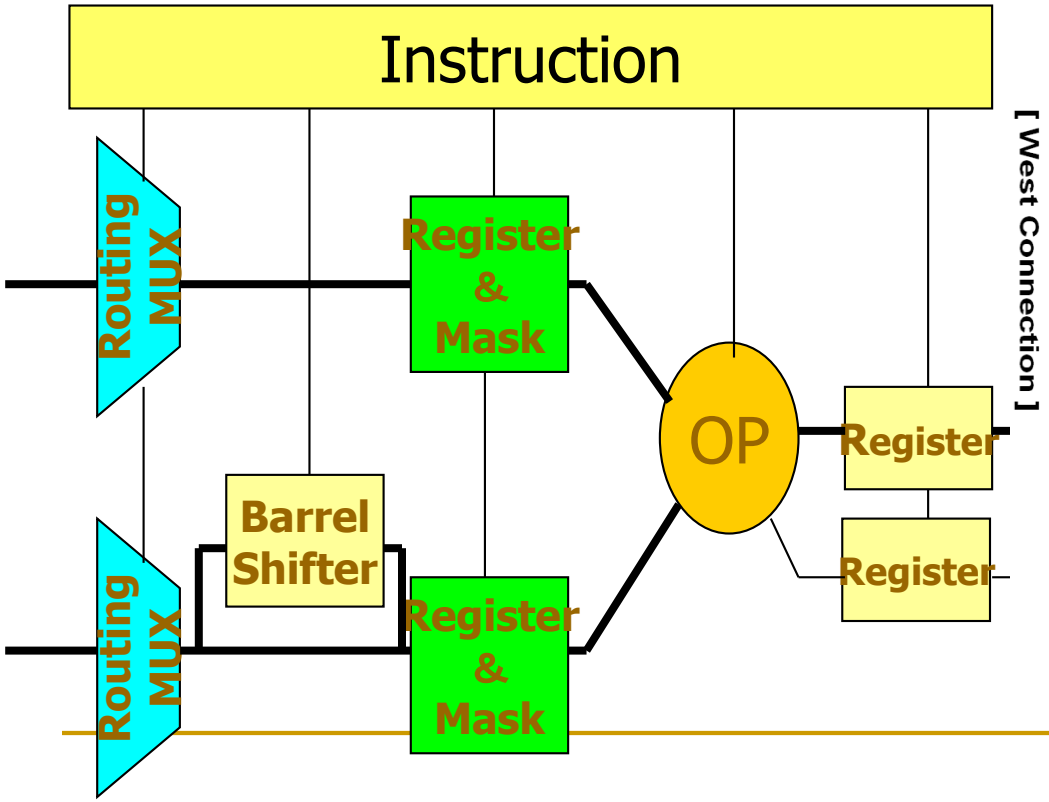
- Coarse Grained Reconfigurable Array (CGRA)
- Parallel processing using a lot of PEs
- Dedicated for stream processing
  - Distributed memory
- High speed dynamic reconfiguration
  - Multicontext
  - Multicast/Broadcast of configuration data inside the chip
  - On-line Configuration
- C-base design

Short history of Dynamically Reconfigurable Processors

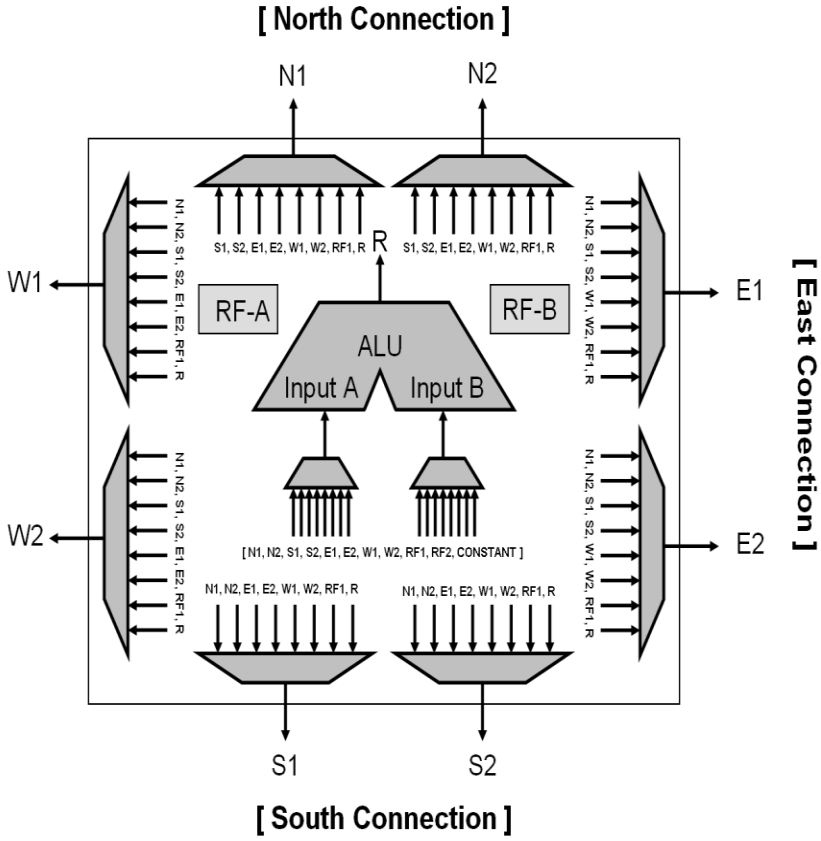


Coarse Grain Structure of PE

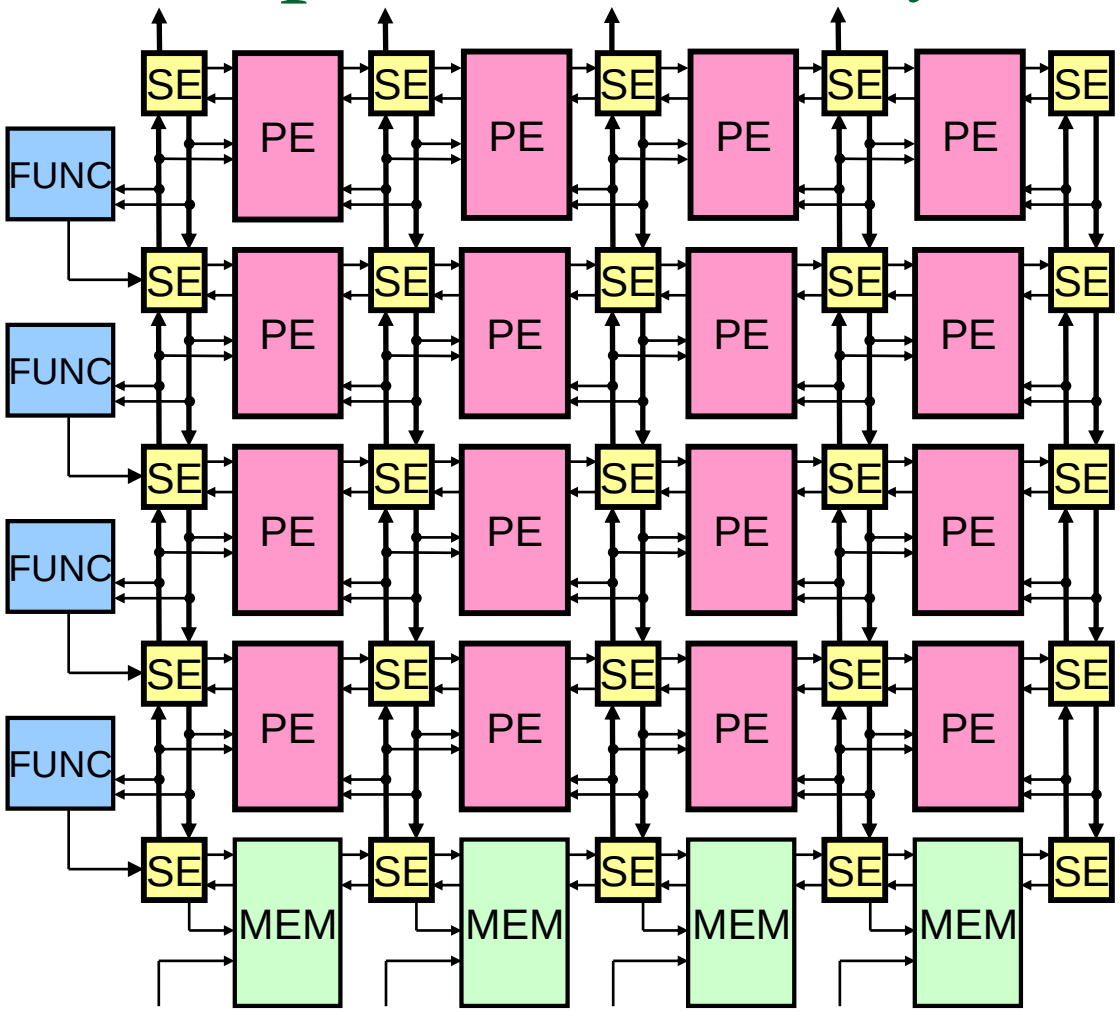
Chameleon CS2112



Kress Array II



An example of PE array



Most of Japanese semiconductor Companies has their own projects! (2009 ASP-DAC Panel)

Product	Vendor	Context	Data	PE
D-Fabric	Panasonic	Deliver	4	Homo
Xpp	PACT	Deliver	24	Homo
S5/S6 engine	Stretch	Deliver	4/8	Hetero
CS2112	Chameleon	Multi-C（8）	16/32	Homo
DAPDNA-2	IPFlex	Multi-C（4）	32	Hetero
DRP-1	NEC electronics	Multi-C（16）	8	Homo
STP-engine	NEC electronics	Multi-C(32)	8	Homo
Kilocore	Rapport	Multi-C	8	Homo
ADRES	IMEC	Multi-C（32）	16	Homo
FE-GA	Hitachi	Multi-C	16	Hetero
For Car-tuners	SANYO	Multi-C(4)	24	Homo
FlexSword(SAKE)	Toshiba	Multi-C(4/16)	16	Homo
Cluster	Fujitsu	Multi-C	16	Hetero

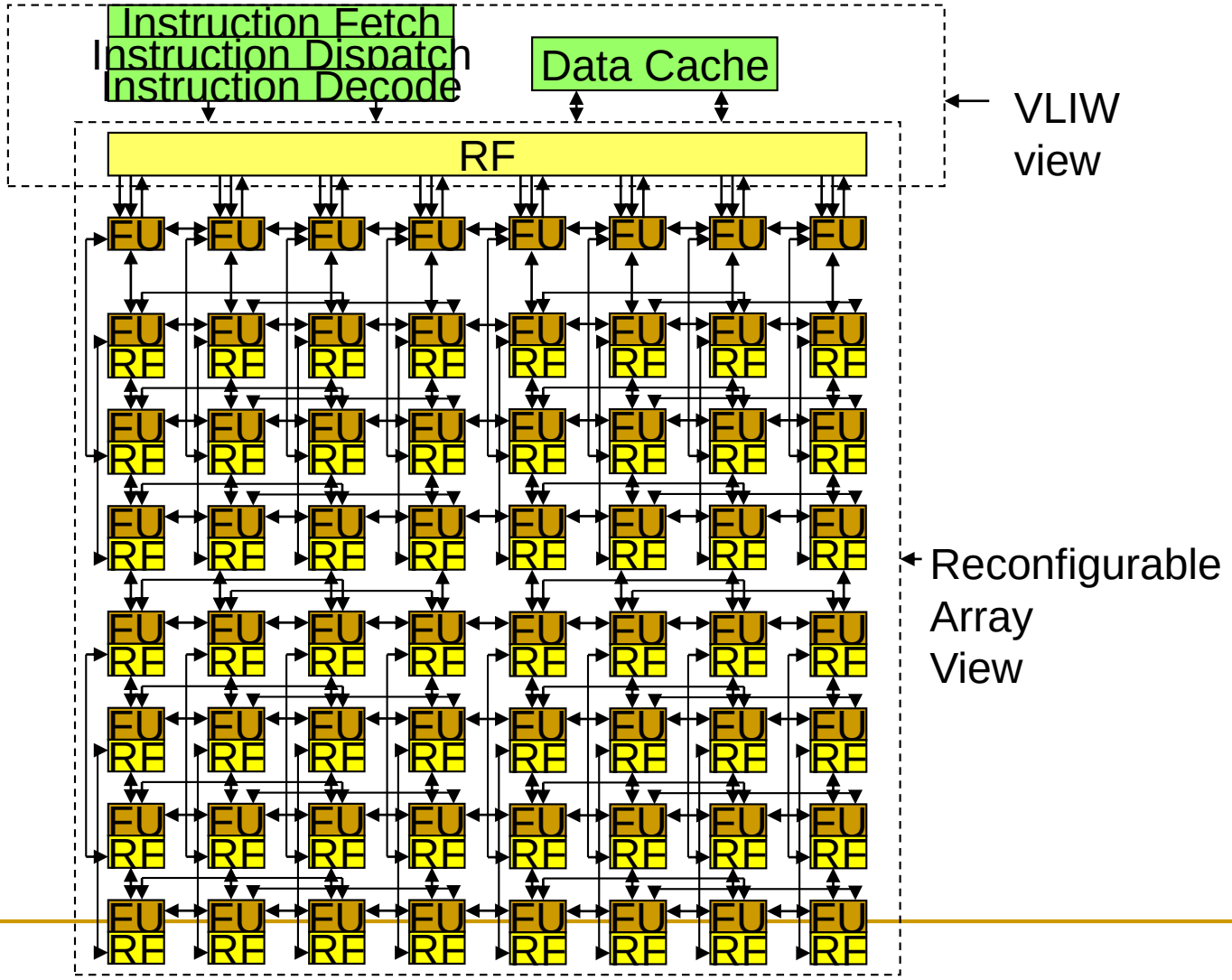
Now most of them disappeared
Shonan Meeting [2012]

Product	Vendor	Context	Data	PE
D-Fabric	Panasonic	Deliver	4	Homo
Xpp	PACT	Deliver	24	Homo
S5/S6 engine	Stretch	Deliver	4/8	Hetero
CS2112	Chameleon	Multi-C（8）	16/32	Homo
DAPDNA-2	IPFlex→Tokyo Keki	Multi-C（4）	32	Hetero
DRP-1	NEC electronics	Multi-C（16）	8	Homo
STP-engine（DRP-2)	Renesas electronics	Multi-C(32)	8	Homo
Kilocore	Rapport	Multi-C	8	Homo
ADRES/SRP	IMEC→Used in Somsung's smart phone	Multi-C（32）	16	Homo
FE-GA	Hitachi	Multi-C	16	Hetero
For Car-tuners	SANYO	Multi-C(4)	24	Homo
FlexSword(SAKE)	Toshiba	Multi-C(4/16)	16	Homo
Cluster	Fujitsu	Multi-C	16	Hetero

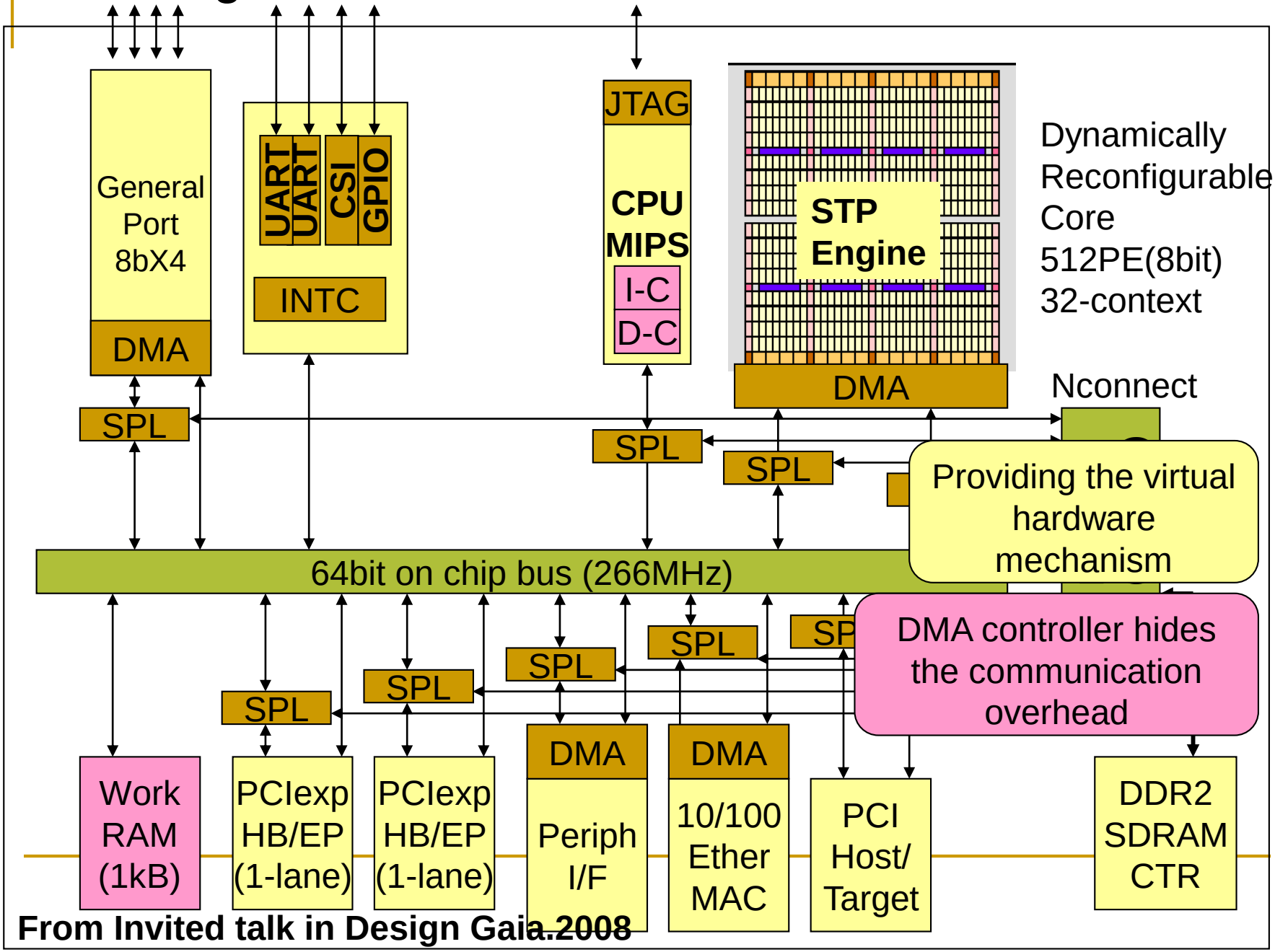
SRP (Samsung Reconfigurable Processor)

- Samsung announced to use widely in their smart phones（ICFPT2012 Seoul）
- Based on IMEC's ADRES
  - High performance architecture with 400MHz-1GHz clock
  - Available as VLIW processors
- Configurable PEs for application
- Sophisticated Design Tools

Base of Samsung Reconfigurable Processor (IMEC ADRES)

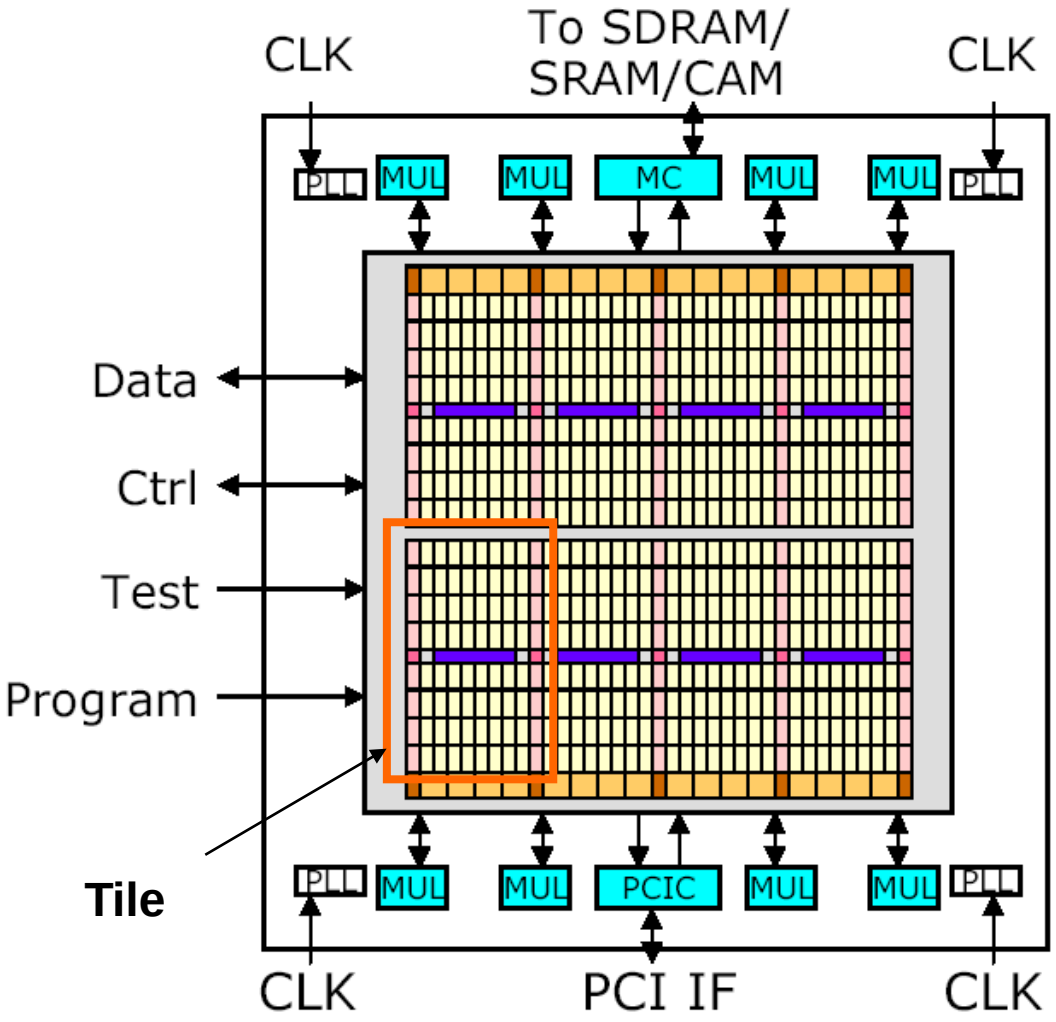


STP engine: Lunesas electronics

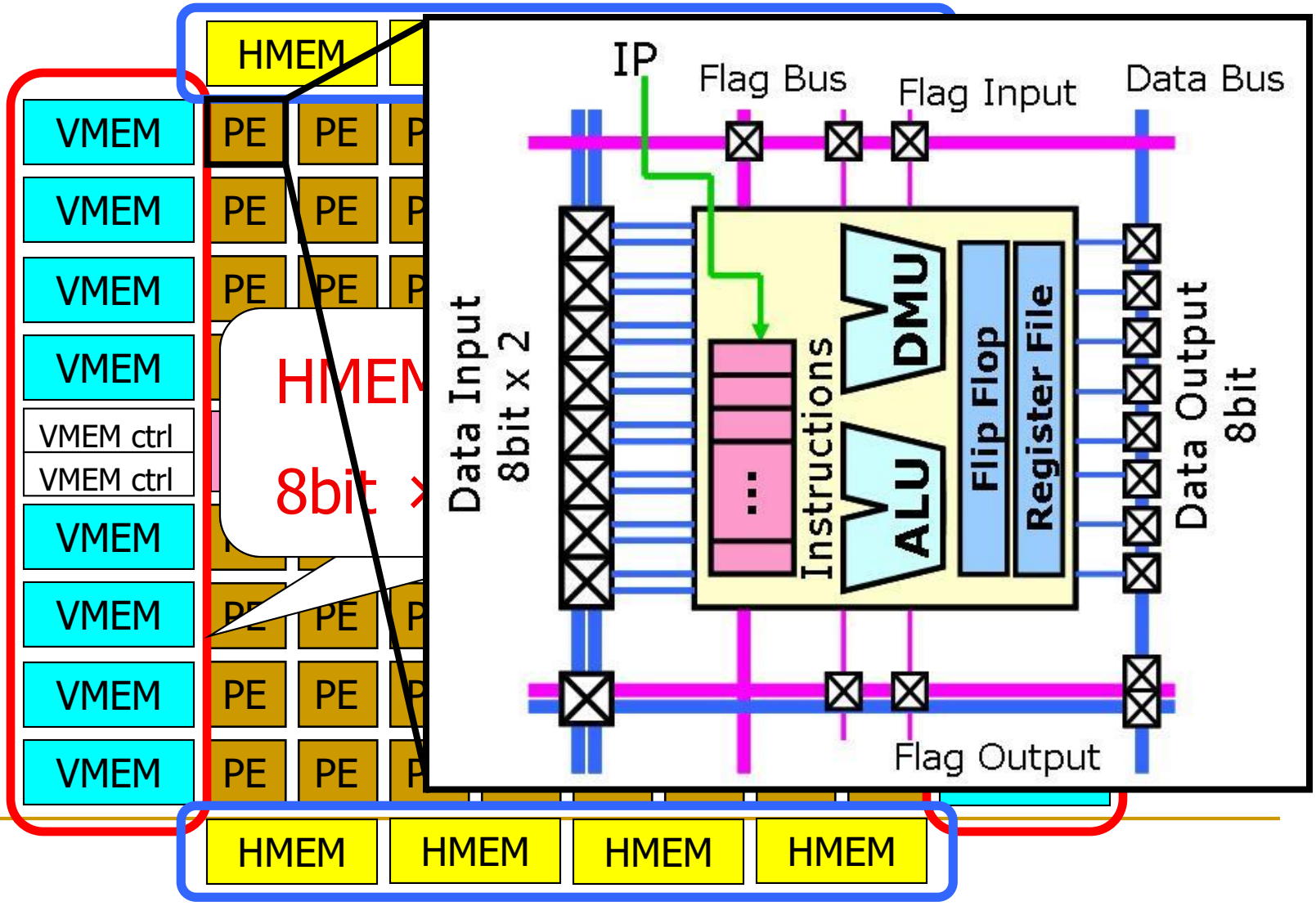


From Invited talk in Design Gaia.2008

DRP (Dynamically Reconfigurable Processor)
A core of STP engine

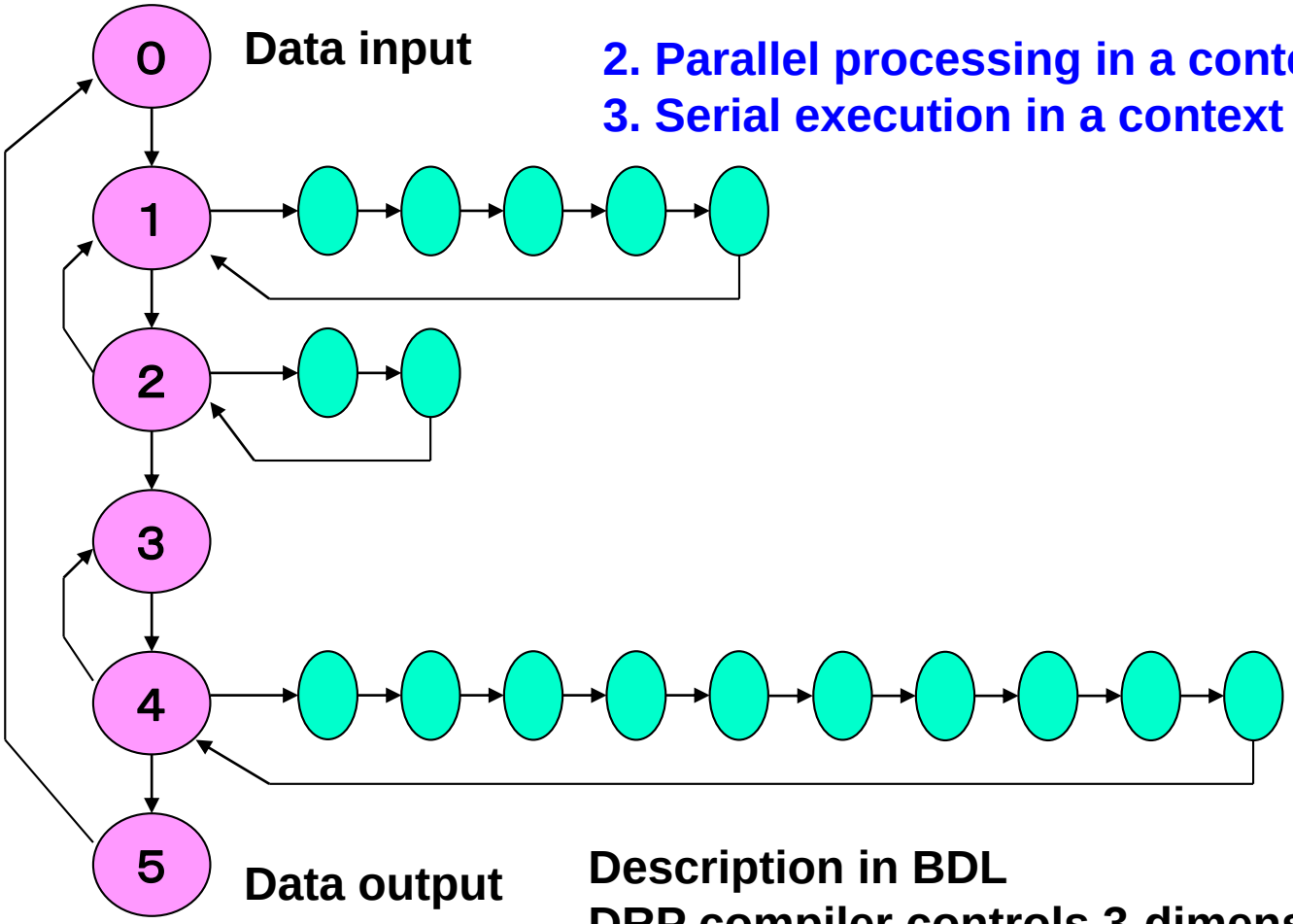


DRP Tile and PE structure



Context control for DRP

1. Context switching



2. Parallel processing in a context
3. Serial execution in a context

Description in BDL
DRP compiler controls 3-dimensional assignment

Main Advantage:
Low power consumption

Why low power ?

1. No redundant hardware
   - There are no instruction fetch mechanisms, cache, TLB, and etc.

   → Of course, it cannot be a general purpose engine, but enough for an accelerator.
   - A bare datapath works only for computation.
2. Parallel Execution with a number of PEs
   - Much lower clock frequency can be used to achieve the same performance as other architectures.
   - The main problem is leakage power, but can be suppressed by power gating techniques.

10X energy efficient compared with DSPs.

5-50X with FPGAs.

Sometimes similar to that for hardwired logic.

Dynamically Reconfigurable Processors

- Coarse grain architecture, somehow like on-chip multiprocessors, while somehow like FPGA.
- Rapidly development from 2001
- They don't find killer application（Chameleon's fail）
- High level language development environment has not been well established.
- A lot of competitors
  - High performance embedded processors
  - Chip multiprocessors
  - Application Specific Configurable Processors
  - DSP
  - Standard FPGA/CPLD
  - System On Chip

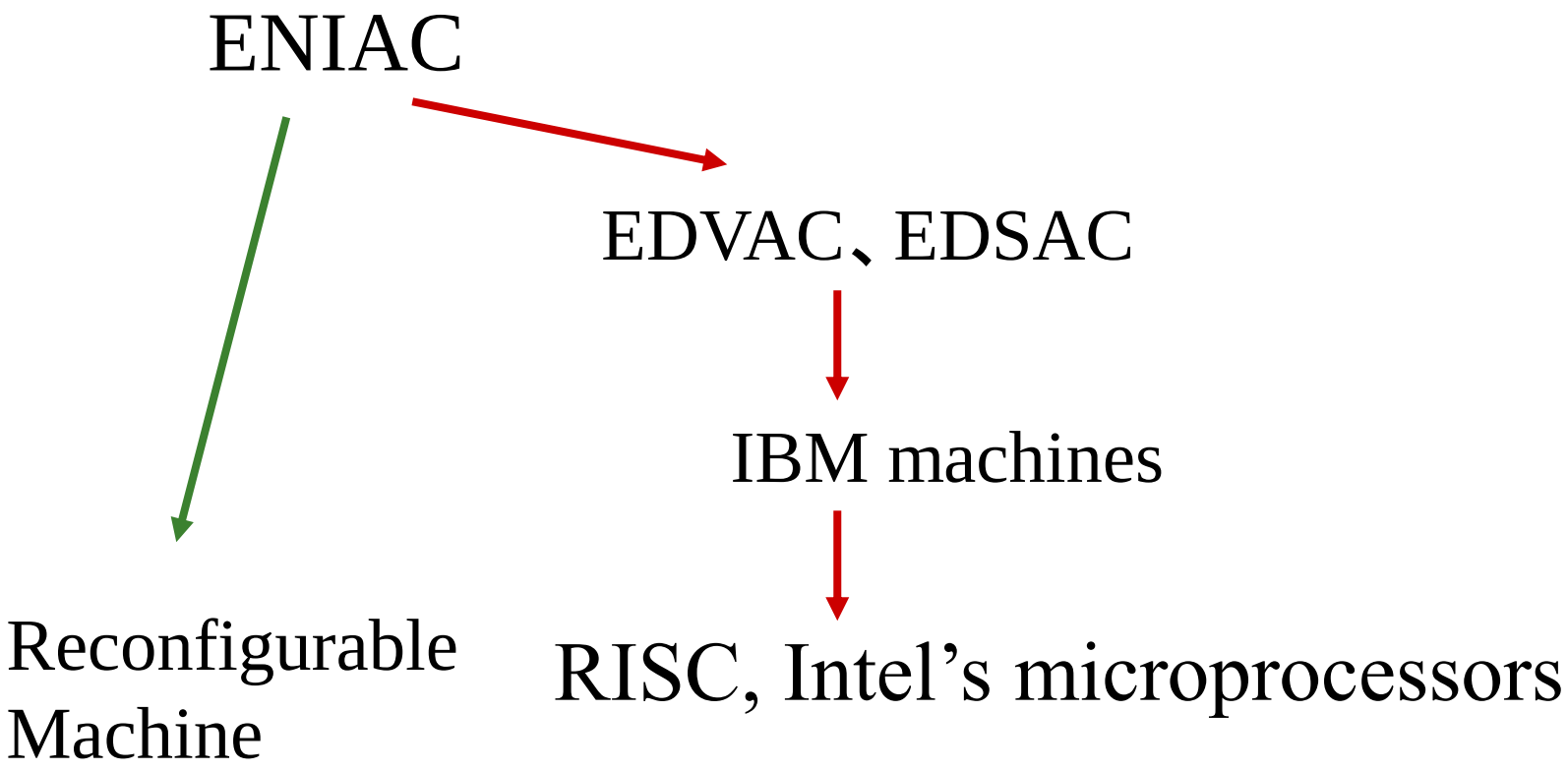
Open Problems

- What's difference between a Program and Configuration Data
  - Reconfigurable Processor Array＝a VLIW machine with an extremely large instructions (Configuration data)
- How frequent should Configuration change?
  - Every-clock-context switching is not advantageous from the viewpoint of consuming power.
  - However, if configuration is rarely switched, dynamic reconfiguration function is useless.
- How is grain size of Processing Element decided？
  - 8-32bit calculators are correct solution?
  - Is it a only escape way from Xilinx's patent ?
- How is the balance between calculators and controllers？
  - Since DRP focuses on calculators, it is difficult to implement complicated control.
  - Does the node balance of ACM correct？

Summary

- Another computing system than stored program computers.
- Not a perfect replace of stored program type computers.
- Advance of the semiconductor techniques directly enhance the performance.
- A lot of problems and subjects to research.

Historical flow of computer systems



Exercise

- There is a systolic array which multiplies 8 x 8 tri-diagonal matrix A with a size 8 vector x. Compute the number of clock cycles for the multiply. Here, the time when the first element of x reaches to the left-most array is assumed to be time 0.