Application-based Performance and Power Analysis of Dynamically Reconfigurable Processor

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Introduction

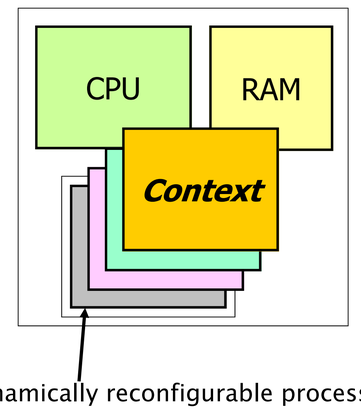
Dynamically reconfigurable processors have three facilities:

- **Coarse-grained processor array architecture**
  8~32-bit processing elements (PEs) and memory modules are laid out in the 2D array, and form a reconfigurable data path called a ***Context***
- **Dynamic reconfigurability**
  - Contexts are dynamically switchable by changing the PE operations and inter-PE connections at run-time
  - Area and power efficiencies will be dramatically improved
- **High-level synthesis technologies for ASIC** are applied and reduce the turn-around time

Dynamically reconfigurable processors are integrated into versatile System-on-Chips (SoCs) and provide high area- and power-efficiency

No one knows how large dynamically reconfigurable processor provides optimal power efficiency for the target application

We have quantitatively evaluated the power efficiency for the target application



Time-multiplexed Execution

Application tasks are divided into multiple steps, and each step is assigned to a context of the DRP Core

Contexts are time-multiplexed and DRP core switches them at run-time

Performance for the target application depends on the way of context scheduling

- The context switching is performed *sequentially*, and
- A lot of PEs and HMEMs/VMEMs in a context are operated *in parallel*

Context Division

- The step which requires a number of PEs are divided into smaller steps
- Although this technique results in increasing the number of context switching, delay and power decrease

Multiple-step-allocation

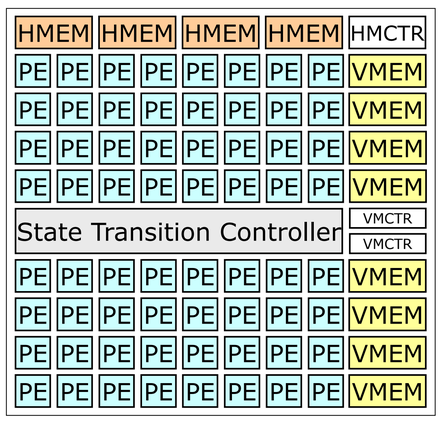
- Steps which require few PEs are assembled to a single context
- Although this technique decreases the number of contexts and improves PE usability, power and delay increase
- Task execution clock cycles are unchanged

The key factor is *Context size* which is defined by the number of available PEs per context

How would the context size affect the power efficiency?

Target Device: DRP Architecture

DRP is an architecture of a coarse grain dynamically reconfigurable processor released by NEC Electronics in 2002.



DRP Tile Architecture

A ***Tile*** is a basic building unit of DRP and consists of

- 8 x 8 8-bit processing elements (PEs)
- 8-bit distributed memory modules (HMEMs/VMEMs)
- VMEM/HMEM controllers (VMCTR/ HMCTR)
- State Transition Controller (STC)

PE has an 8-bit *ALU*, *DMU,* register file (*RFU*), and flip-flop (*FFU*). These units are connected with each other by programmable wires specified by instructions.

Each PE has 16-depth instruction memories (i.e. 16 contexts) and their instruction pointers are delivered from the STC.

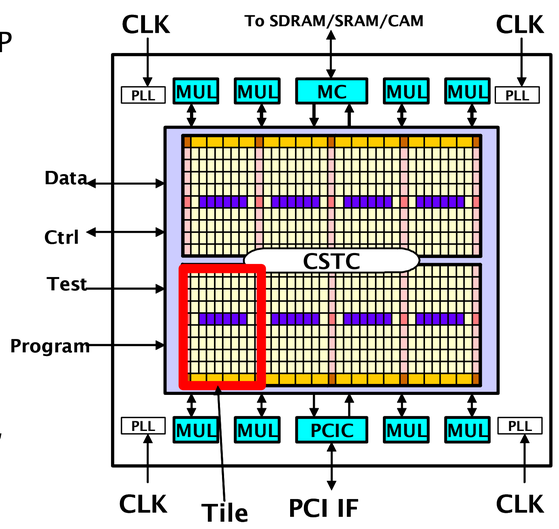
The context switching is able to be performed cycle by cycle.

Multiple Tiles form a desirable-scale DRP Core for the target applications

DRP-1 is a first implementation of DRP

- DRP Core with 4 x 2 Tiles (512 PEs)
- 80 VMEMs and 32 HMEMs
- 8 32-bit Multipliers
- PCI Controller
- External Memory Controller
- Central STC (CSTC)

The integrated design environment, Musketeer, is available

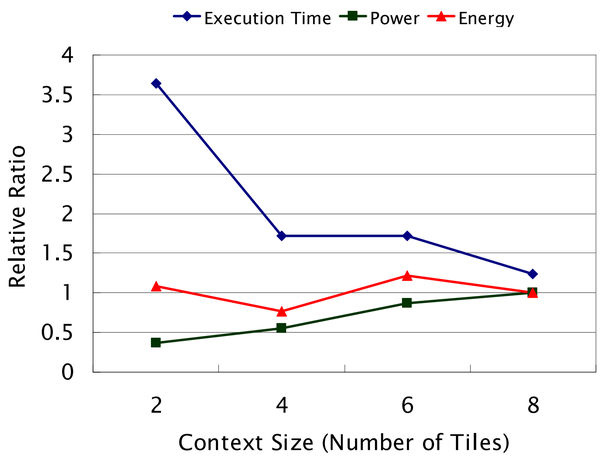


Evaluation Results

We have implemented many stream applications with various context sizes.

Target Applications:
DCT(JPEG Codec), IMDCT (MP3 decoder), FFT, ADPF, AES-ECB, Viterbi Decoder, and SHA-1

DCT



DCT *is a highly parallel application (Max PE number = 293)*

If the context size becomes larger,

- The execution time is grossly reduced
- Power dissipation and energy consumption increase slowly

The power is 302mW at 8 Tiles, and 111mW at 2 Tiles

The most power-efficient context size is 4 Tiles

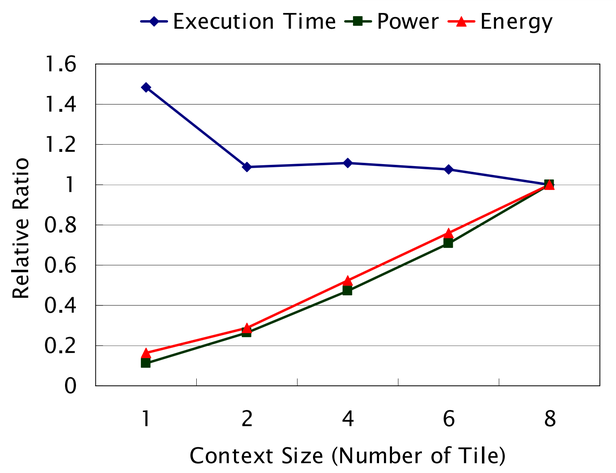
SHA-1

SHA-1 *is small and sequential (Max PE number = 65)*

If the context size becomes larger,

- The 2-Tile case is upper bound of the performance improvement
- Power dissipation and energy consumption increase linearly

The most power-efficient context size is only 1 Tile



The context size with the best cost-performance results in the optimal energy consumption for most applications

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